

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No.09/167,174
Priority Filing Date October 6, 1998
Inventor..... Aftab Ahmad, et al.
Assignee..... Micron Technology, Inc.
Priority Group Art Unit2811
Priority ExaminerO. Nadav
Attorney's Docket No.MI22-1885
Title: Semiconductor Transistor Devices and Methods for Forming Semiconductor
Transistor Devices

PRELIMINARY AMENDMENT

To: Box PATENT APPLICATION
Assistant for Patents and Trademarks
Washington, D.C. 20231

From: James E. Lake (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
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AMENDMENTS

In the Specification

At p. 1, before the "Technical Field" section, insert

--RELATED PATENT DATA

This patent resulted from a continuation application of U.S. Patent Application
Serial No. 09/167,174, filed on October 6, 1998.--

At pg. 36, ln. 12, replace "93" with --293--.

At pg. 36, ln. 3, replace "307" with --311--.

At pg. 36, ln. 5, replace "307" with --311--.

At p. 93, replace the "Abstract" with,

EL 844053675

--ABSTRACT OF THE DISCLOSURE

In one aspect, the invention encompasses a transistor device comprising a region of a semiconductor material wafer, and a transistor gate over a portion of the region. The transistor gate has a pair of opposing sidewalls which are a first sidewall and a second sidewall. The device further comprises a pair of opposing sidewall spacers adjacent the sidewalls of the transistor gate and a pair of opposing first conductivity type source/drain regions within the semiconductor material wafer proximate the transistor gate. One of the sidewall spacers extends along the first sidewall of the gate and the other of the sidewall spacers extends along the second sidewall of the gate. The entirety of the semiconductor wafer material under one of the sidewall spacers being defined as a first segment of the semiconductor wafer material, and the entirety of the semiconductor wafer material which is under the other of the sidewall spacers being defined as a second segment of the semiconductor wafer material. The first and second segments of the semiconductor material wafer are separated from the first and second source/drain regions by first and second gap regions, respectively, of the semiconductor material wafer. The device further comprises a pair of opposing second conductivity type halo regions within the first and second gap regions.--.

In The Claims

Please cancel claims 1-98 without prejudice, and add new claims 99-115.

99. (New claim) A semiconductor transistor structure comprising:

a region of a semiconductor wafer;

a gate over the region, the gate having first and second sidewalls;

first conductivity type heavily doped first and second source/drain regions

proximate the first and second sidewalls, respectively;

first and second oxide layers extending along and at least partially covering the first and second sidewalls, respectively;

first and second sidewall spacers extending along and at least partially covering the first and second oxide layers, respectively, the entirety of the semiconductor wafer under the first and second sidewall spacers being defined as first and second segments, respectively, and the first and second segments being separated from the respective first and second source/drain regions by respective first and second gaps, no part of the first and second gap regions being under the respective first and second sidewall spacers; and

second conductivity type halo regions within the first and second gap regions and not extending into the first and second segments.

100. (New claim) The structure of claim 99 wherein the first and second sidewall spacers comprise silicon nitride.

101. (New claim) The structure of claim 99 wherein one of the first and second conductivity types is n-type and the other is p-type.

102. (New claim) The structure of claim 99 wherein the halo regions extend directly under a full lateral extent of the first and second source/drain regions.

103. (New claim) The structure of claim 99 wherein the first and second sidewalls are opposing sidewalls.

104. (New claim) The device of claim 99 wherein the first and second gap regions are not under any sidewall spacer.

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105. (New claim) A semiconductor transistor device comprising:

a transistor gate over a semiconductor material wafer, the transistor gate having opposing first and second sidewalls;

first conductivity type, heavily doped, first and second opposing source/drain regions within the semiconductor material wafer beside the respective first and second sidewalls;

first and second opposing oxide layers extending along and covering the respective first and second sidewalls;

first and second opposing sidewall spacers extending along and at least partially covering the respective first and second oxide layers;

first and second opposing segments consisting of an entirety of the semiconductor wafer material under the respective first and second sidewall spacers, the first and second segments being separated from the first and second source/drain regions by respective first and second gap regions of the semiconductor material wafer;

second conductivity type, first and second opposing halo regions within the respective first and second gap regions; and

one of the first and second conductivity types being n-type and the other of the first and second conductivity types being p-type.

106. (New claim) The device of claim 105 wherein the first and second halo regions extend directly under a full lateral extent of the respective first and second source/drain regions.

107. (New claim) The device of claim 105 wherein the first and second halo regions do not extend into the respective first and second segments.

108. (New claim) The device of claim 105 wherein the first and second oxide layers extend laterally out from the respective first and second sidewalls, directly under the respective first and second sidewall spacers, and directly over the respective first and second segments.

109. (New claim) The device of claim 108 wherein the first and second oxide layers further extend past the respective first and second sidewall spacers, directly over the respective first and second gap regions, and directly over at least a portion of the respective first and second source/drain regions.

110. (New claim) The device of claim 109 wherein the first and second oxide layers further extend to a full lateral extent of the first and second source/drain regions.

111. (New claim) The device of claim 105 wherein the first and second gap regions are not under any sidewall spacer.

112. (New claim) A semiconductor transistor structure comprising:

a region of a semiconductor wafer;

a gate over the region, the gate having first and second opposing sidewalls;

first conductivity type heavily doped first and second opposing source/drain

regions proximate the first and second sidewalls, respectively;

first and second opposing oxide layers extending along and at least partially covering the first and second sidewalls, respectively;

first and second sidewall opposing spacers extending along and at least partially covering the first and second oxide layers, respectively, the entirety of the semiconductor wafer under the first and second sidewall spacers being defined as first and second segments, respectively, and the first and second segments being separated from the respective first and second source/drain regions by respective first and second gaps, no part of the first and second gap regions being under the respective first and second sidewall spacers; and

second conductivity type halo regions within the first and second gap regions and not extending into the first and second segments, wherein one of the first and second conductivity types is n-type and the other is p-type.

113. (New claim) The structure of claim 112 wherein the first and second sidewall spacers comprise silicon nitride.

114. (New claim) The structure of claim 112 wherein the halo regions extend directly under a full lateral extent of the first and second source/drain regions.

115. (New claim) The device of claim 112 wherein the first and second gap regions are not under any sidewall spacer.

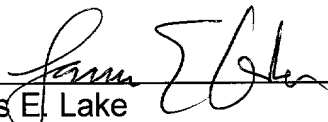
REMARKS

Claims 1-98 are canceled. New claims 99-115 are pending in the application.

Examination of claims 99-115 is requested.

Respectfully submitted,

Dated: 29 Nov 2001

By: 
James E. Lake
Reg. No. 44,854

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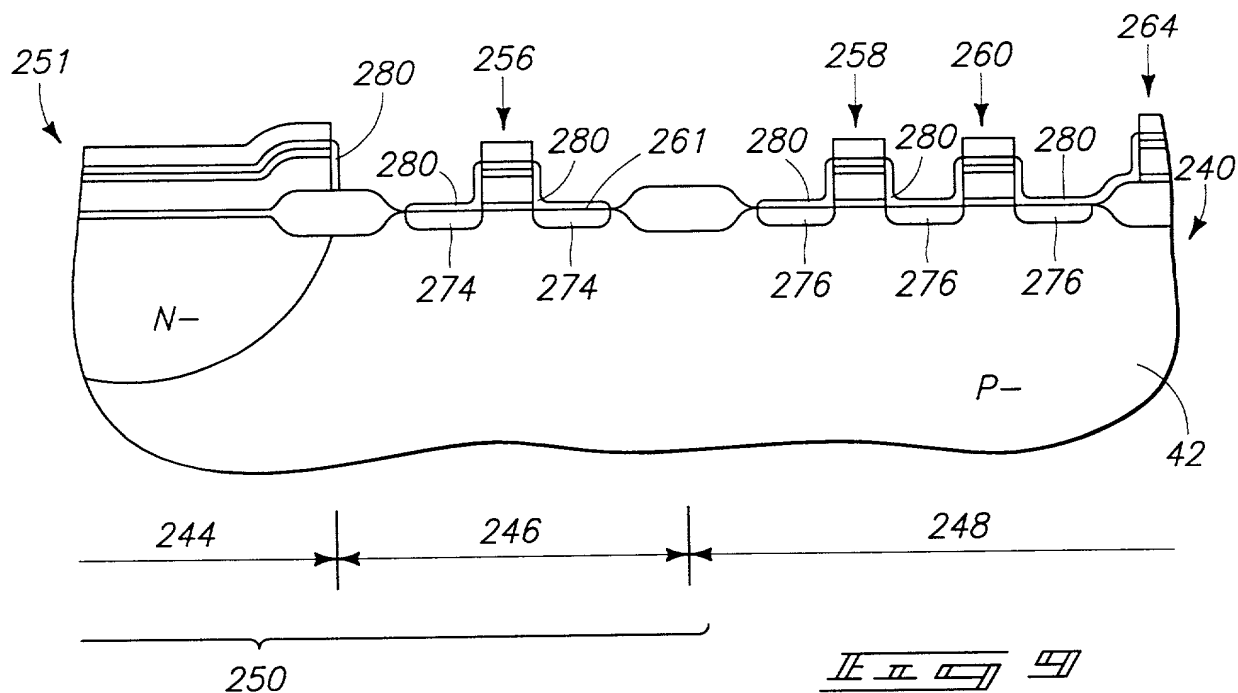


FIG. 9
PRIOR ART

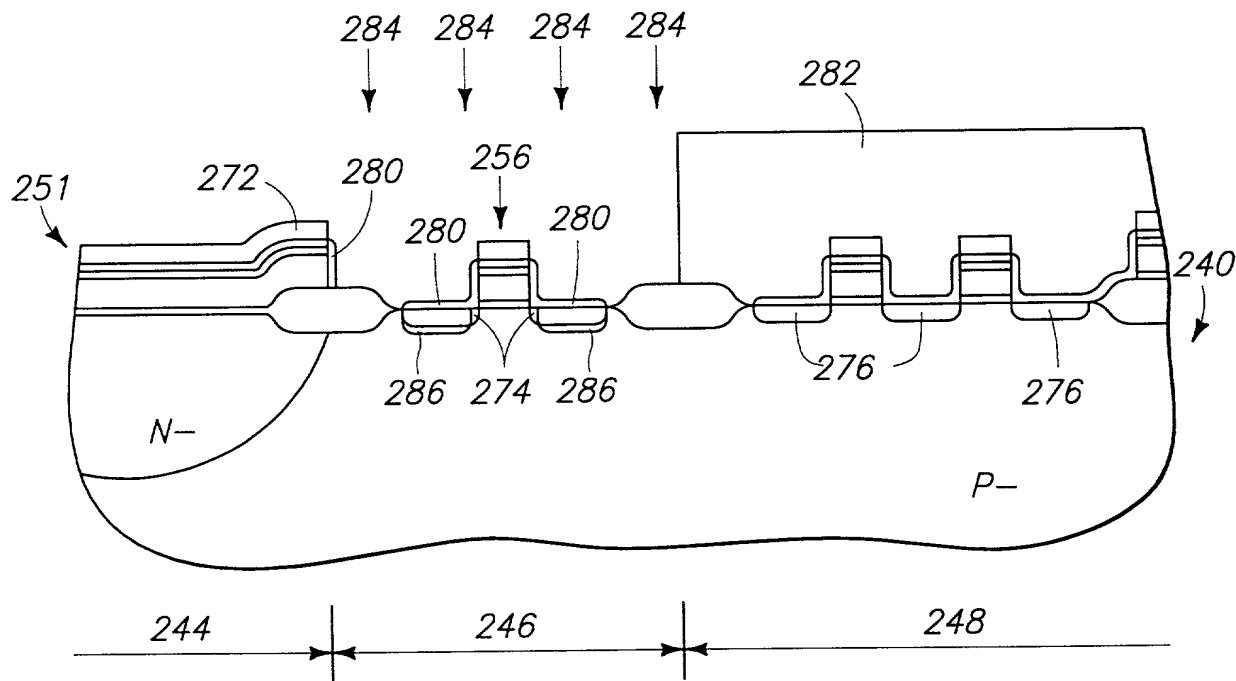


FIG. 10
PRIOR ART

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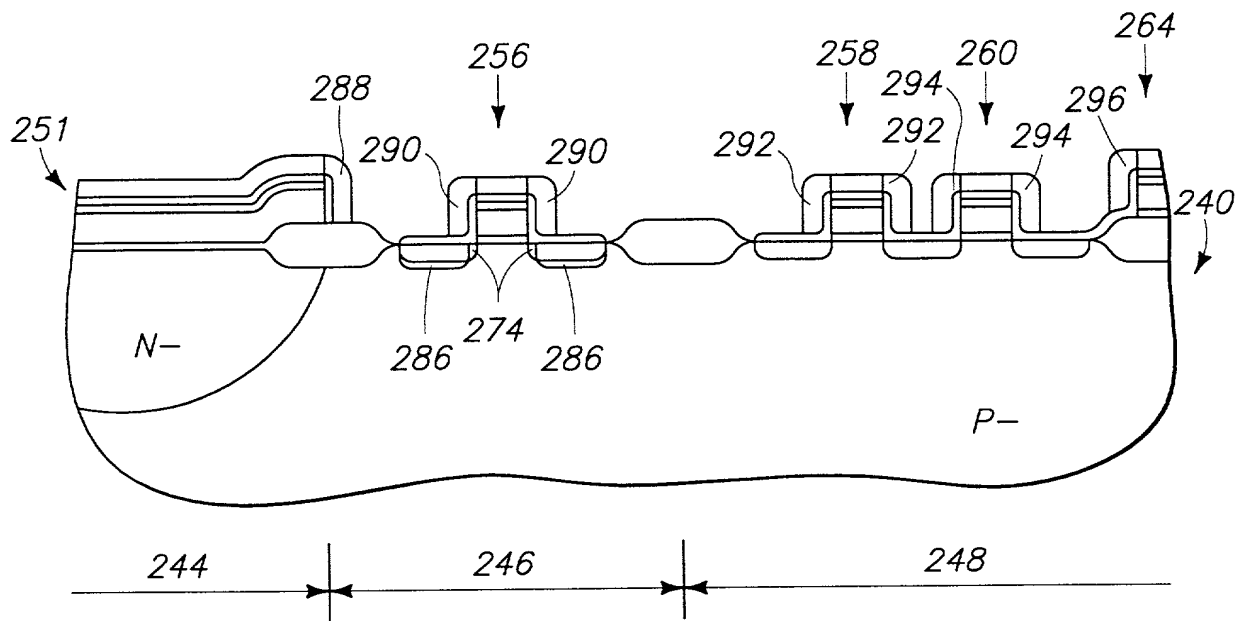


FIG 11
PRIOR ART

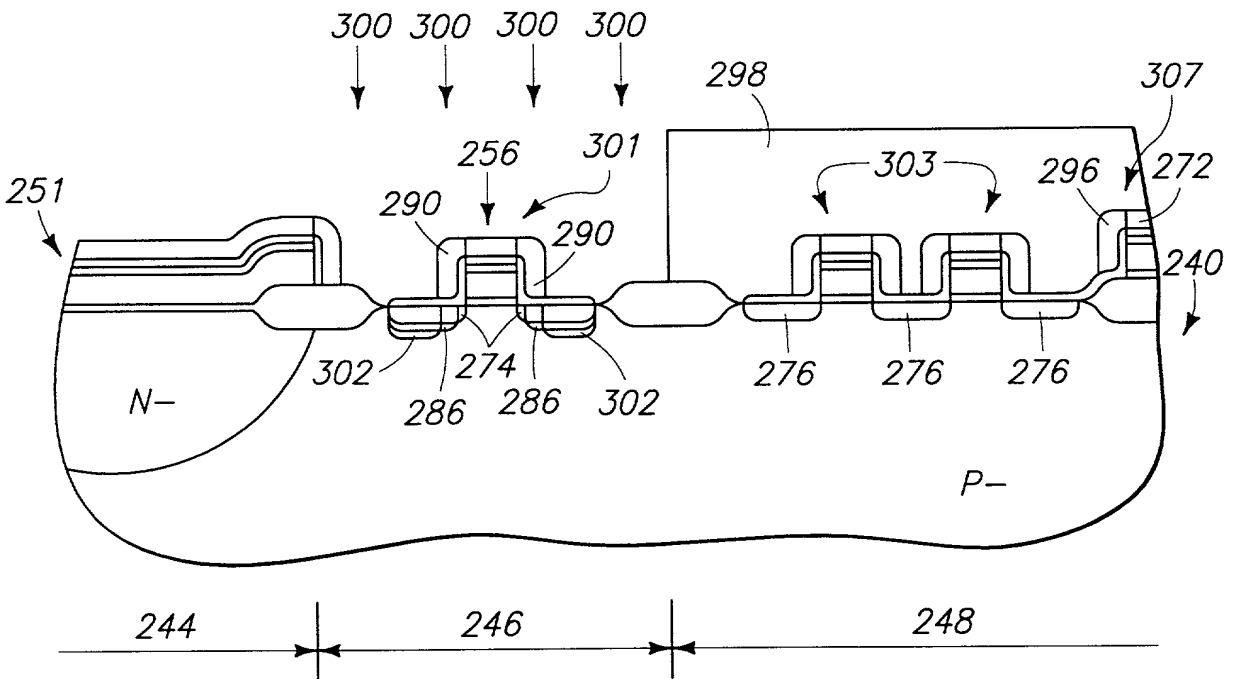
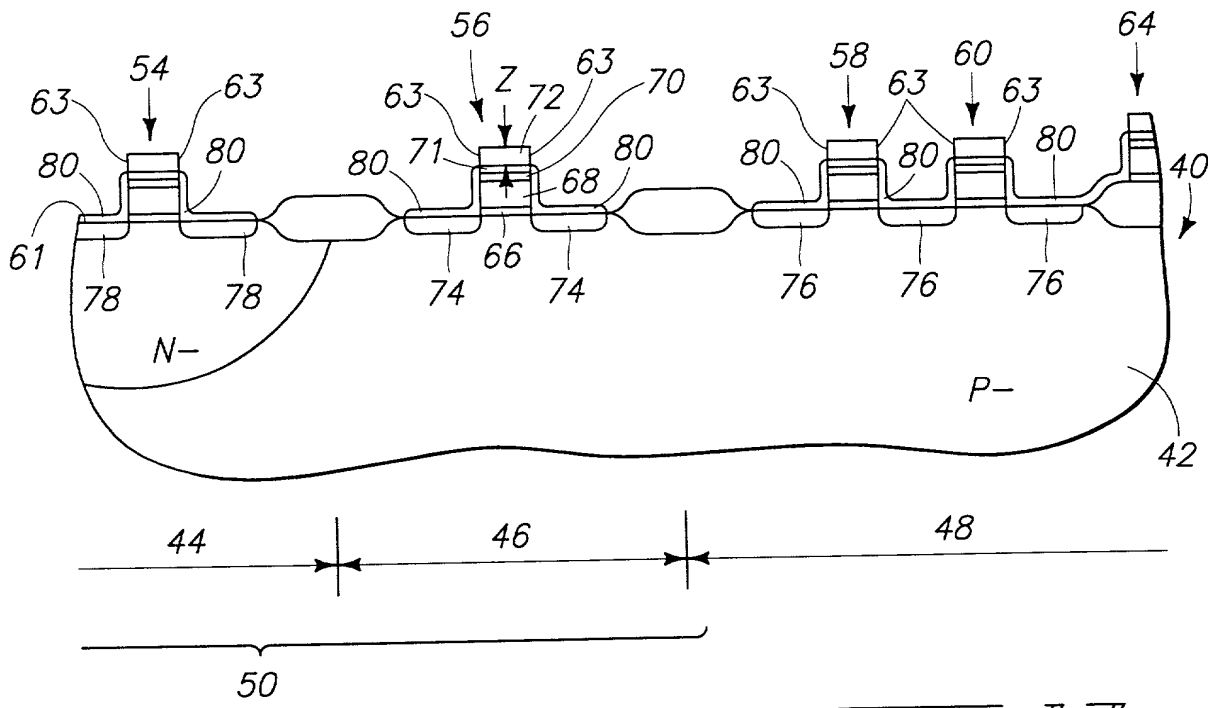
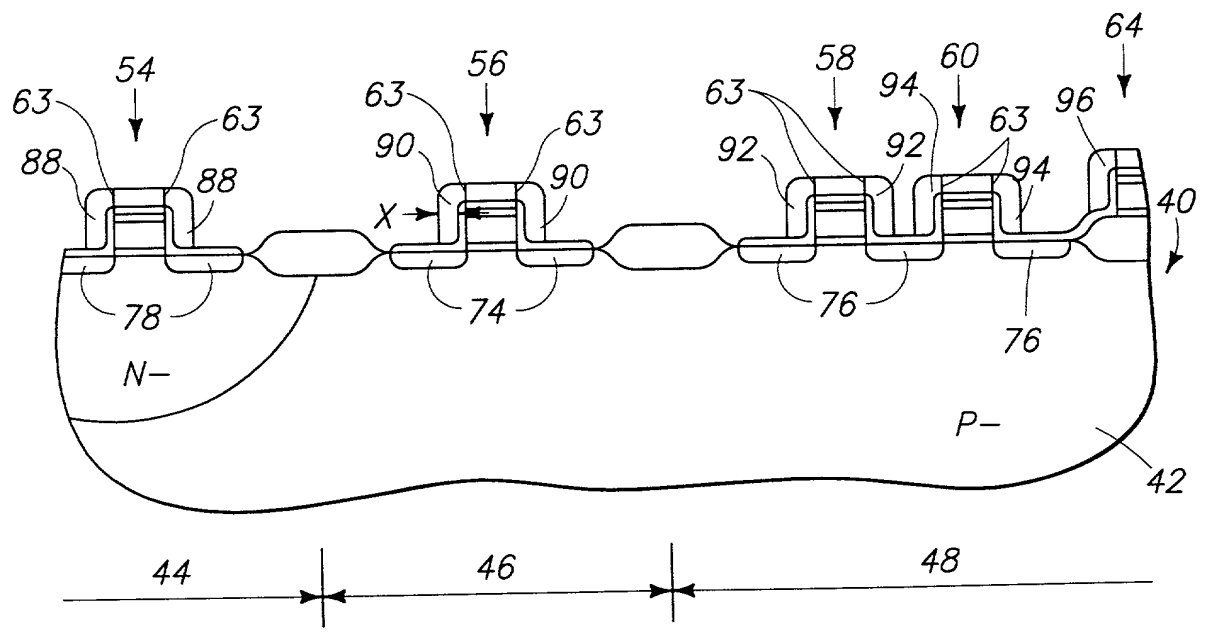


FIG 12
PRIOR ART

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II II II II II

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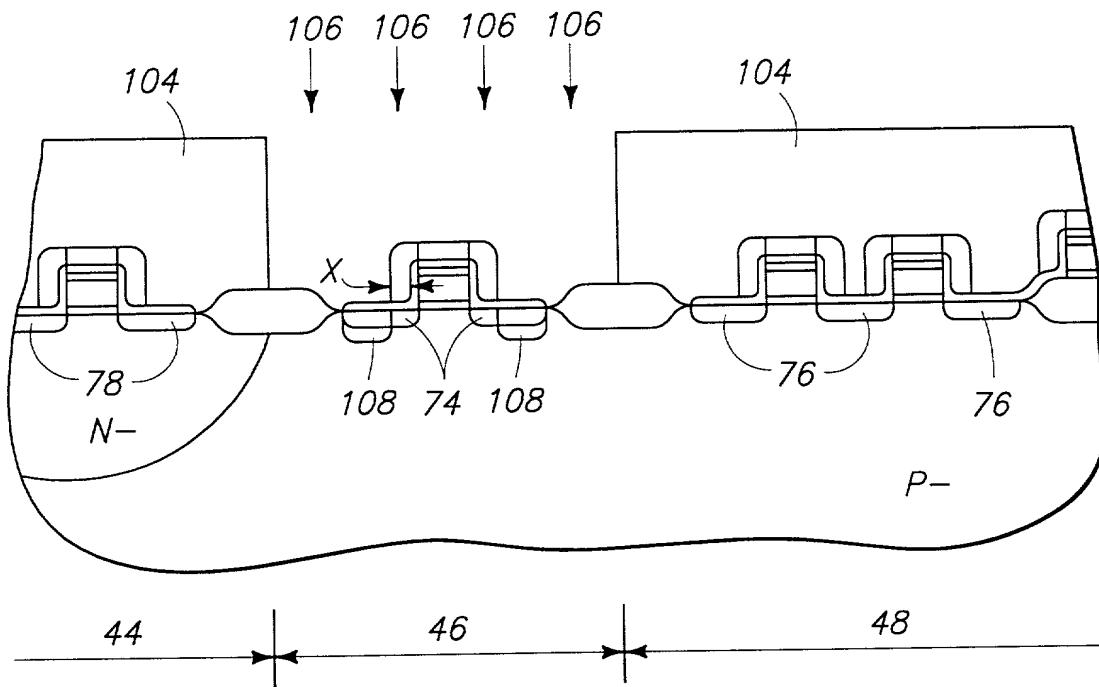


Fig. 115

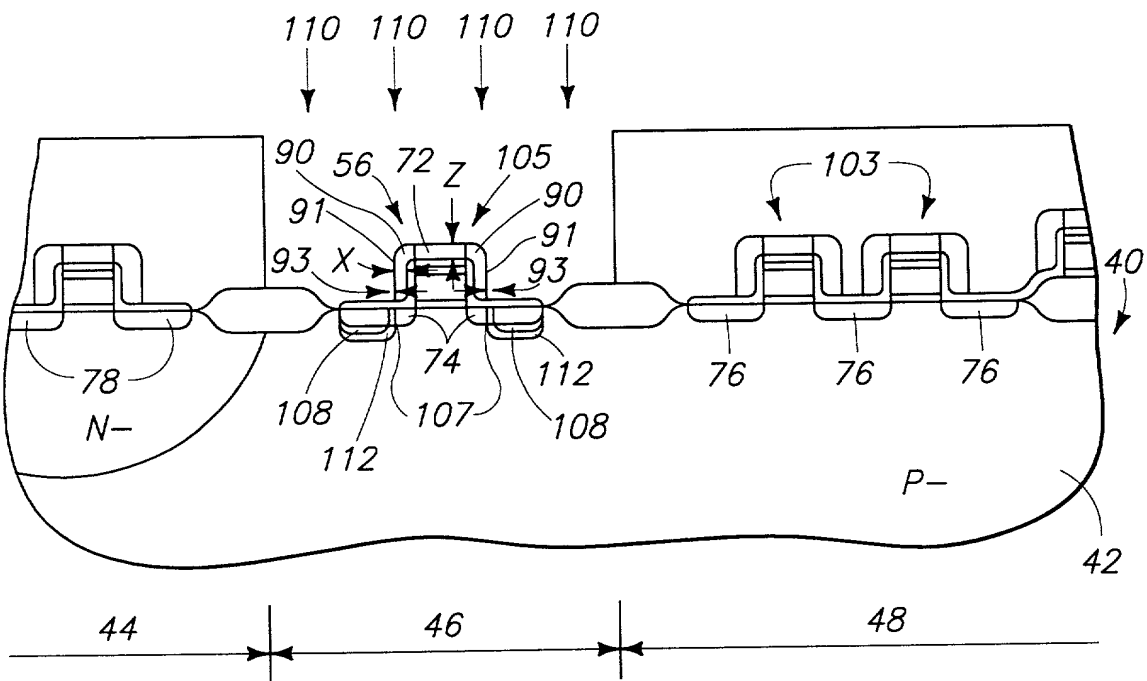
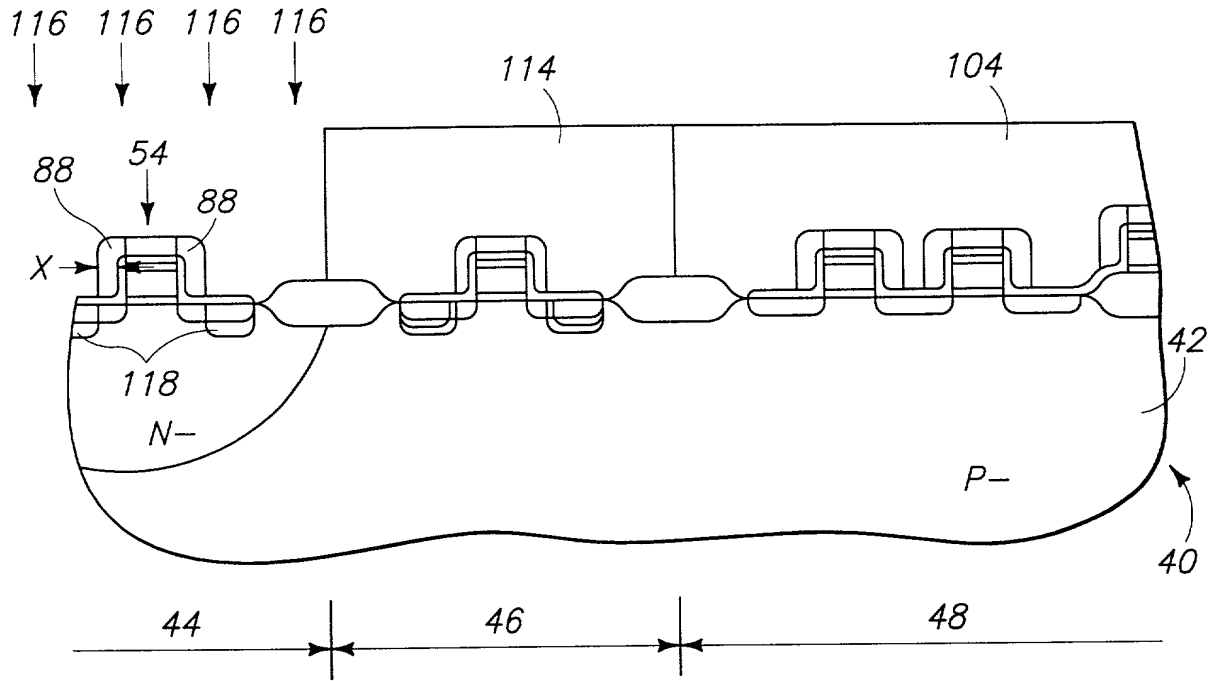
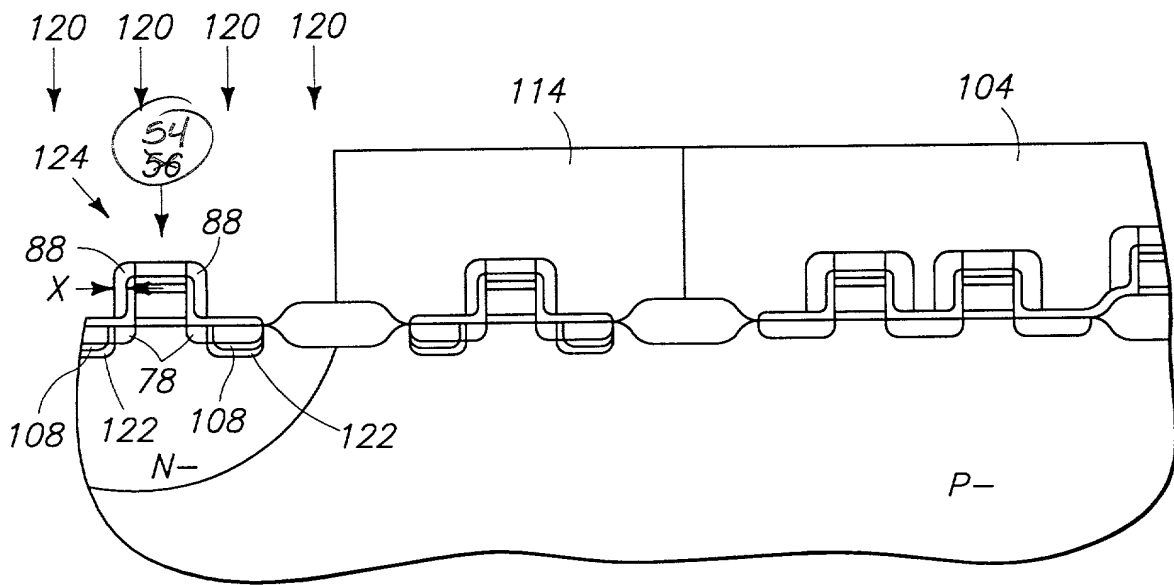


Fig. 116

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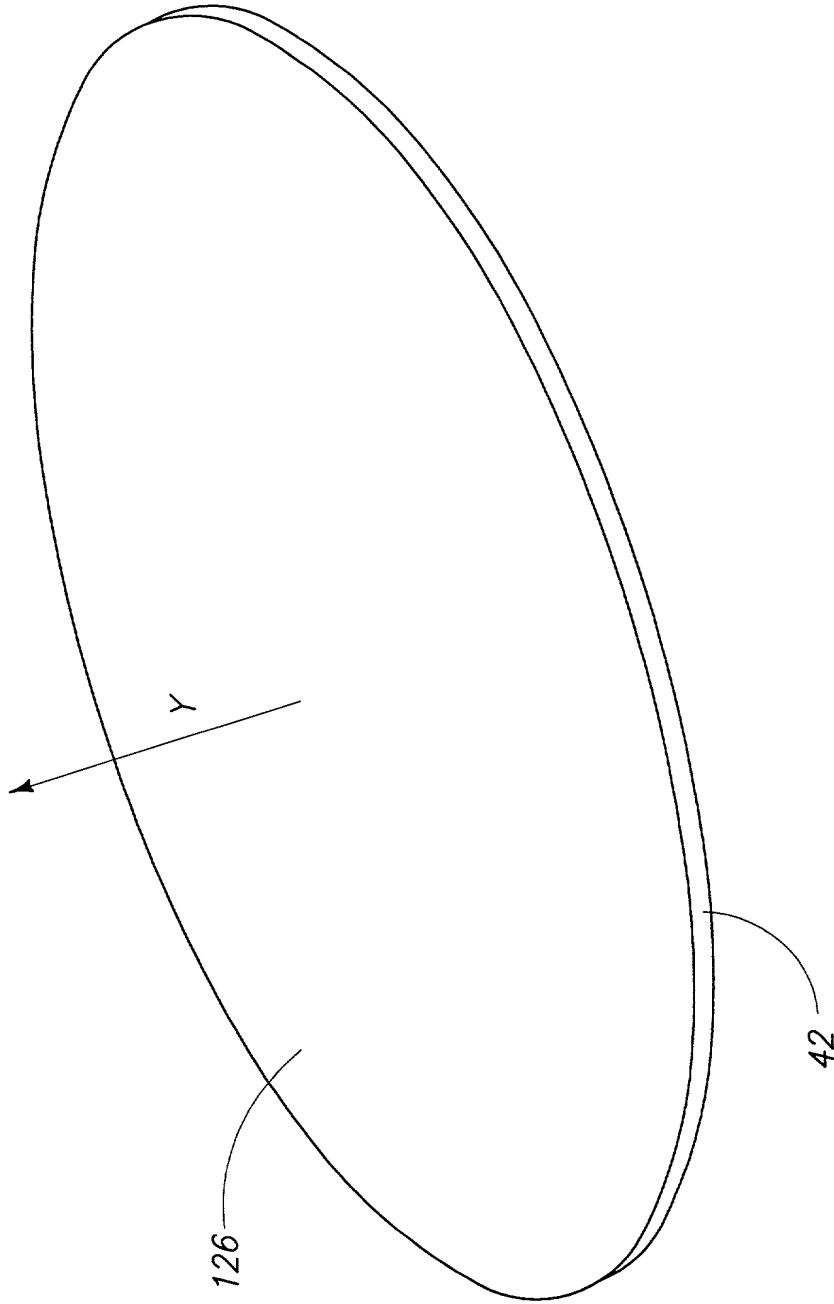


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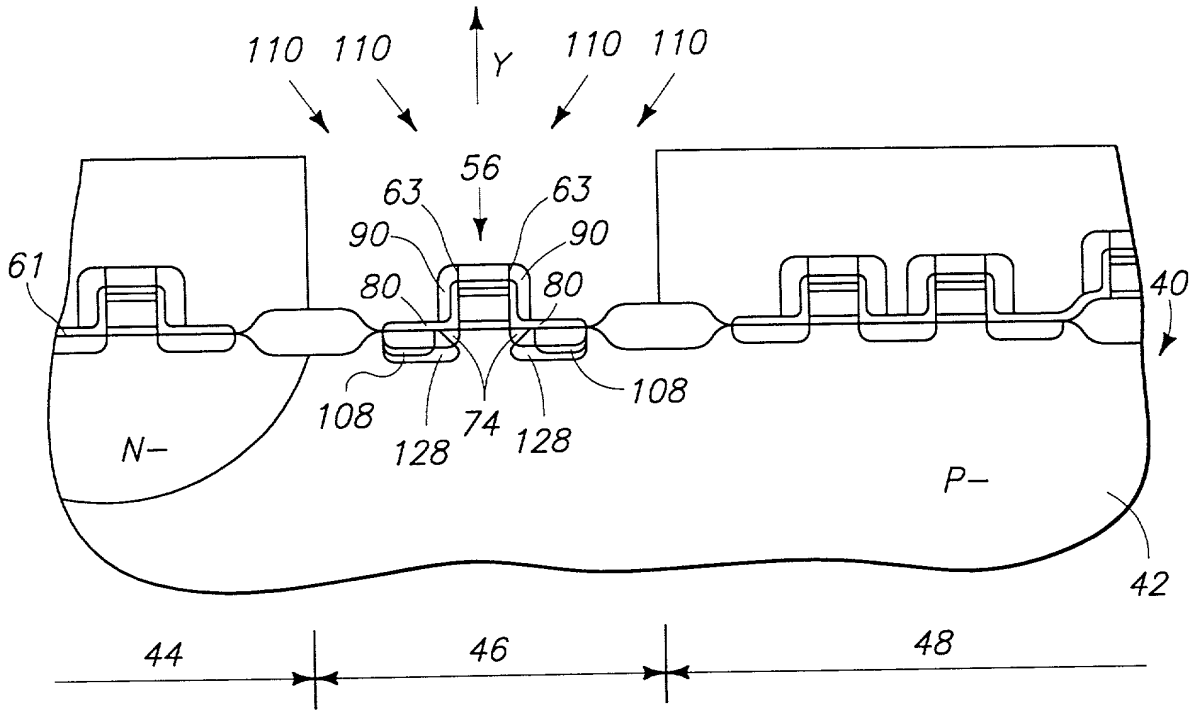
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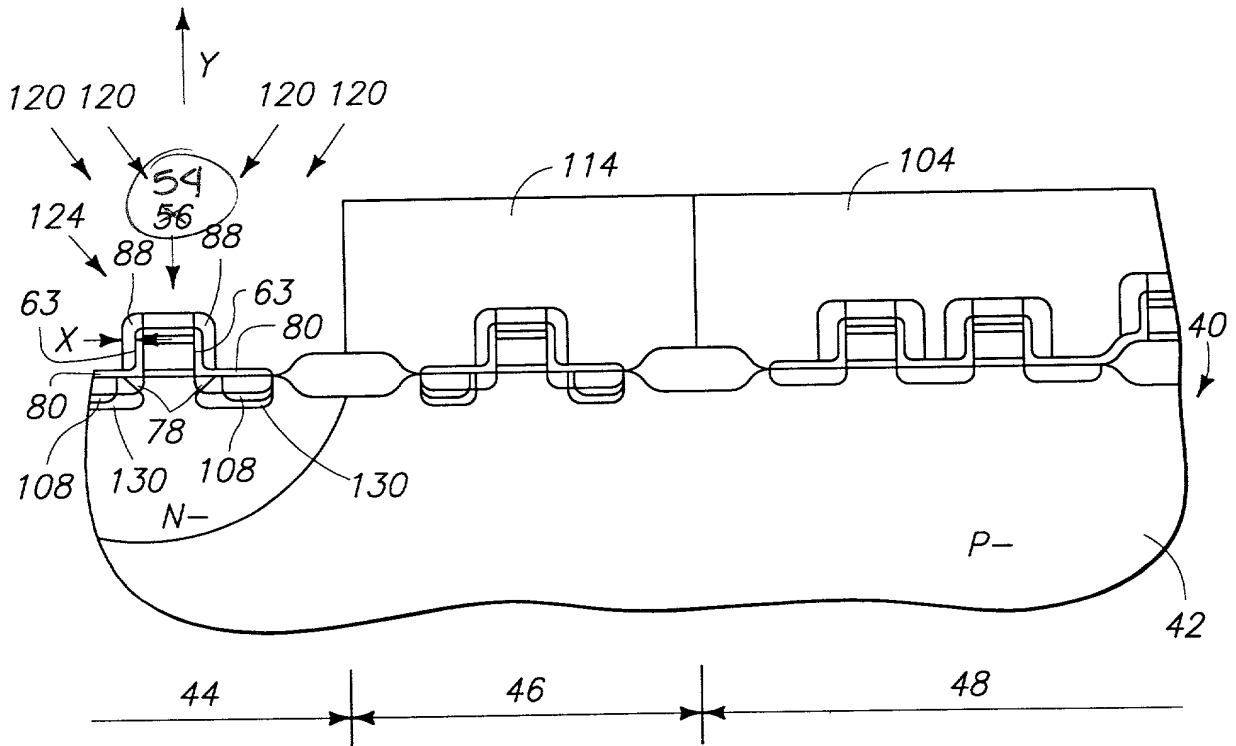


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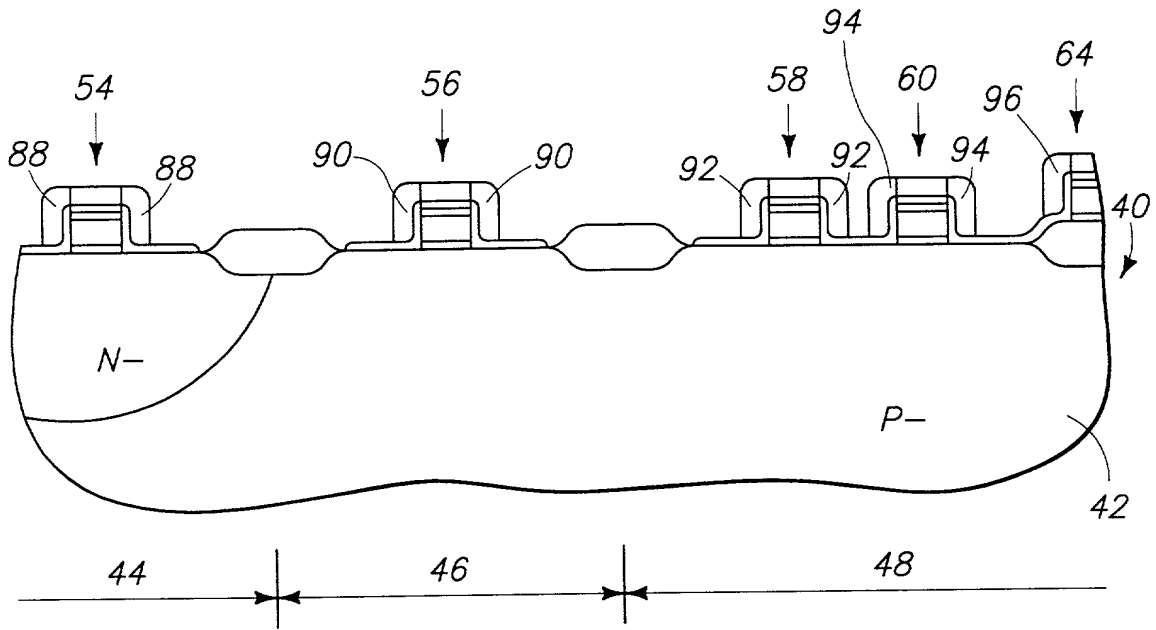


Fig. 22

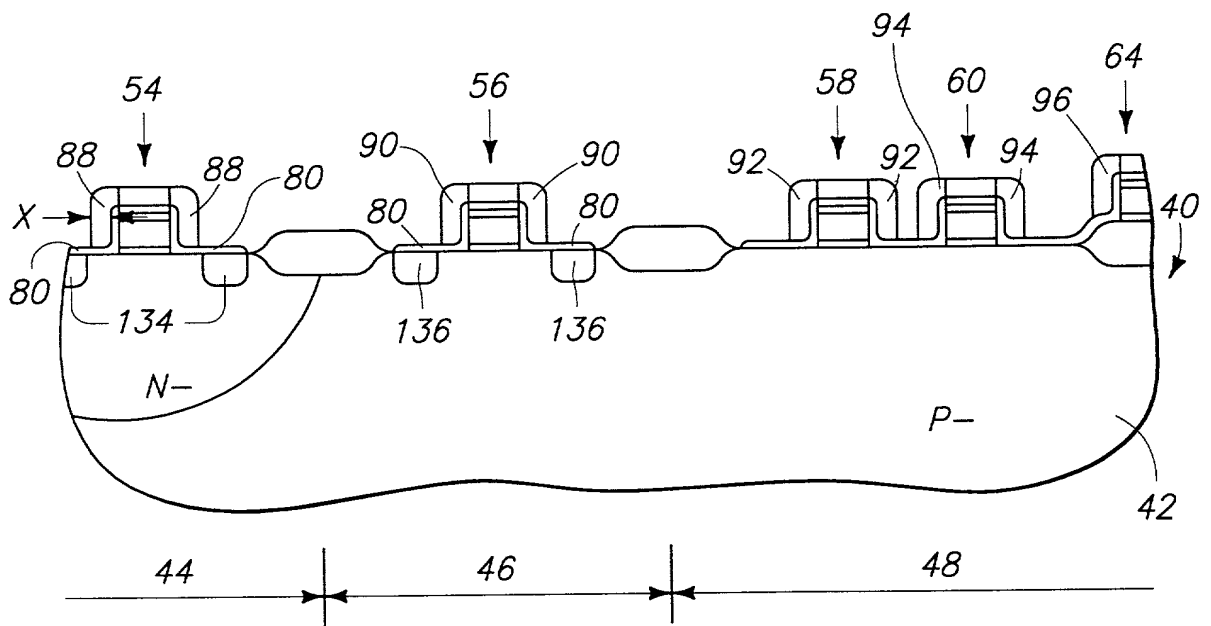
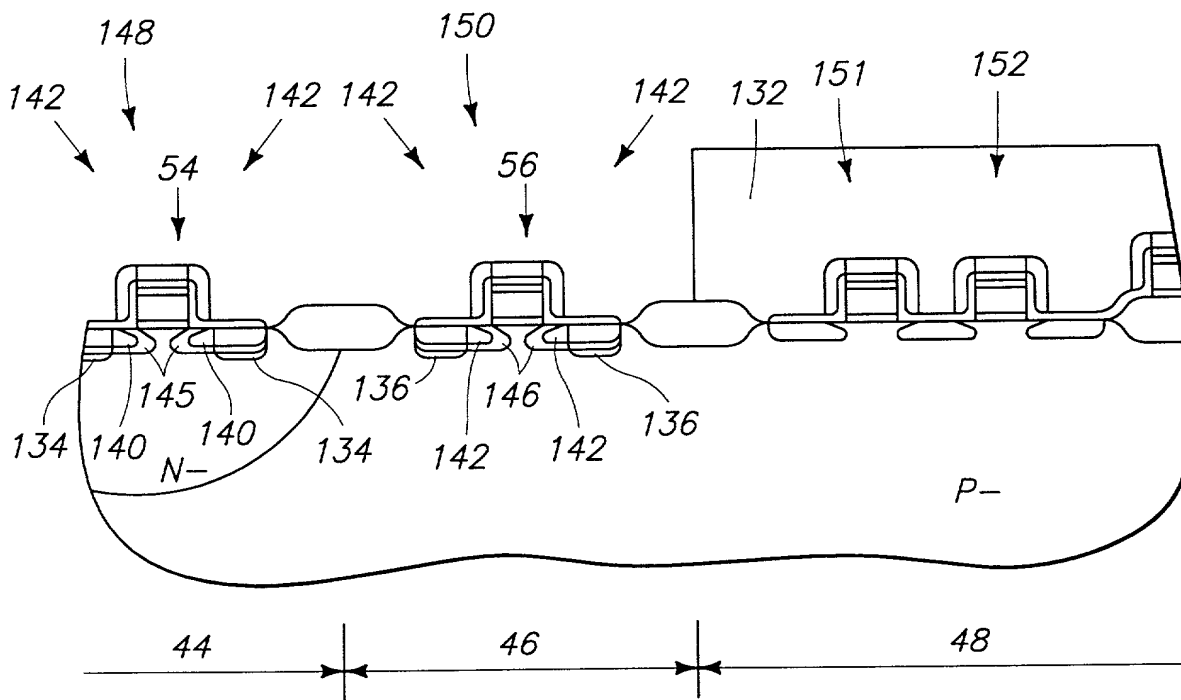
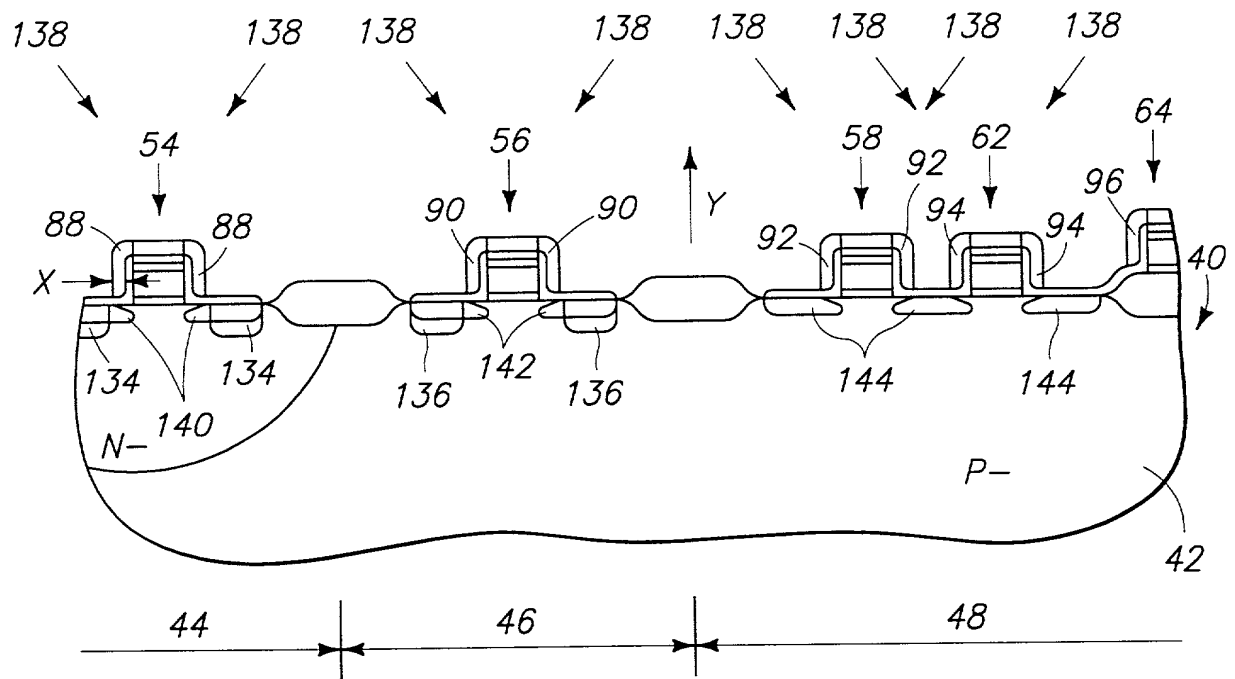
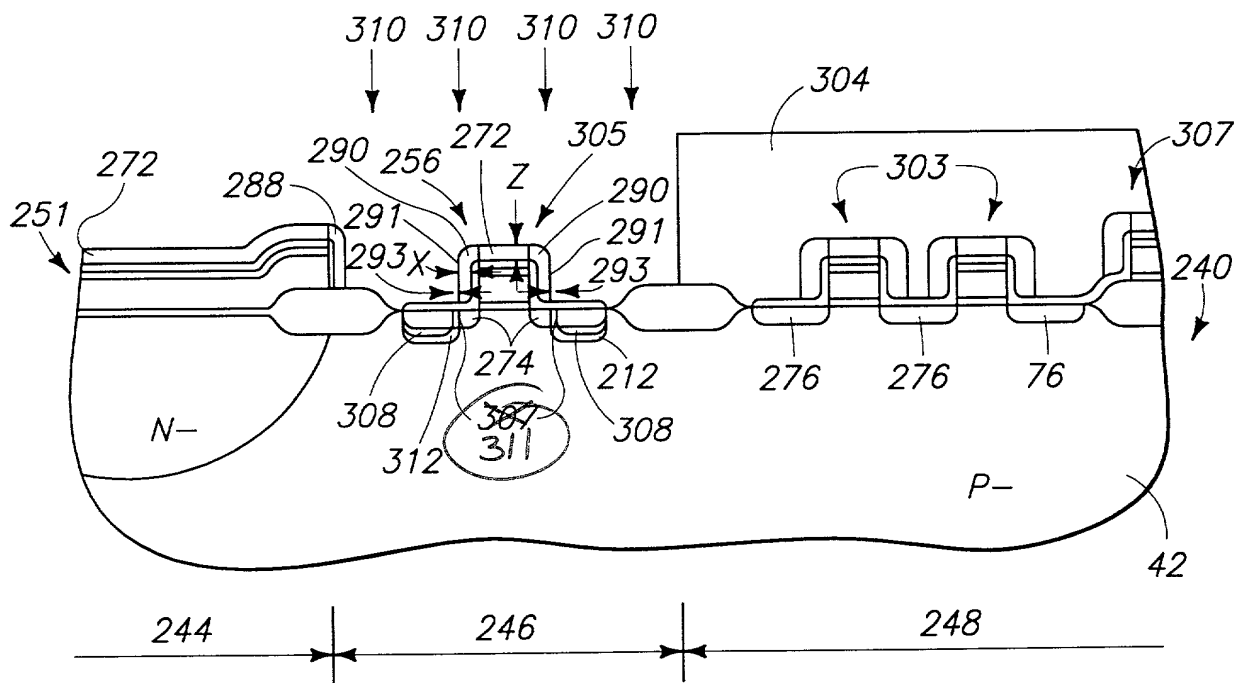
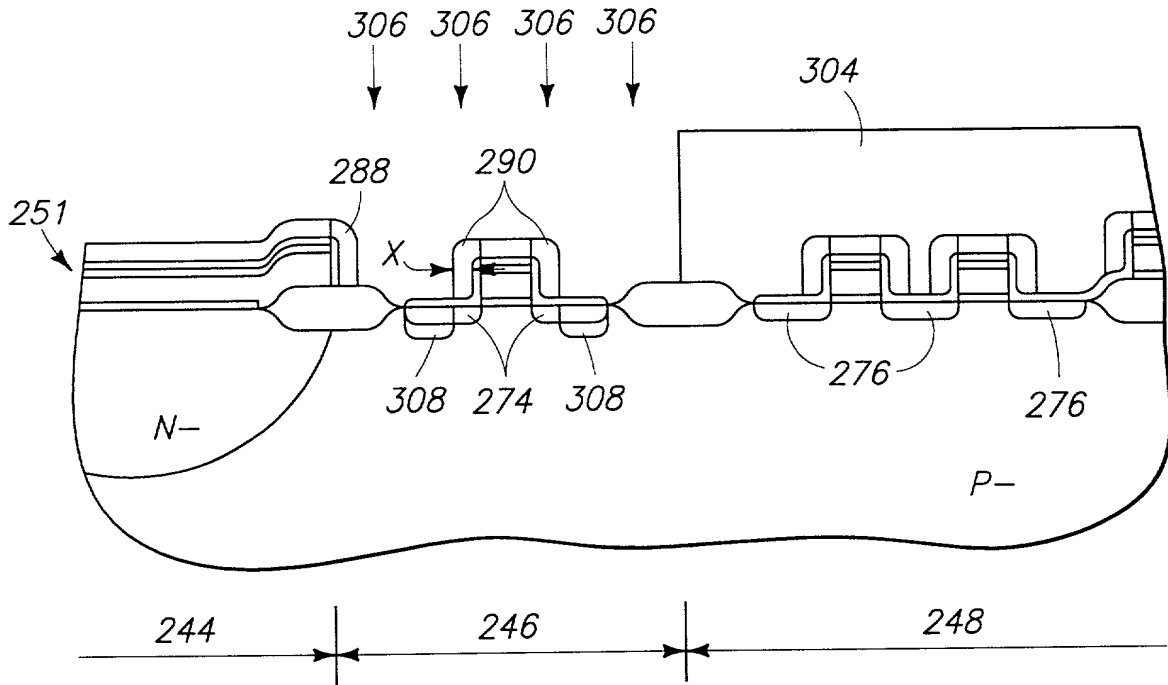


Fig. 23

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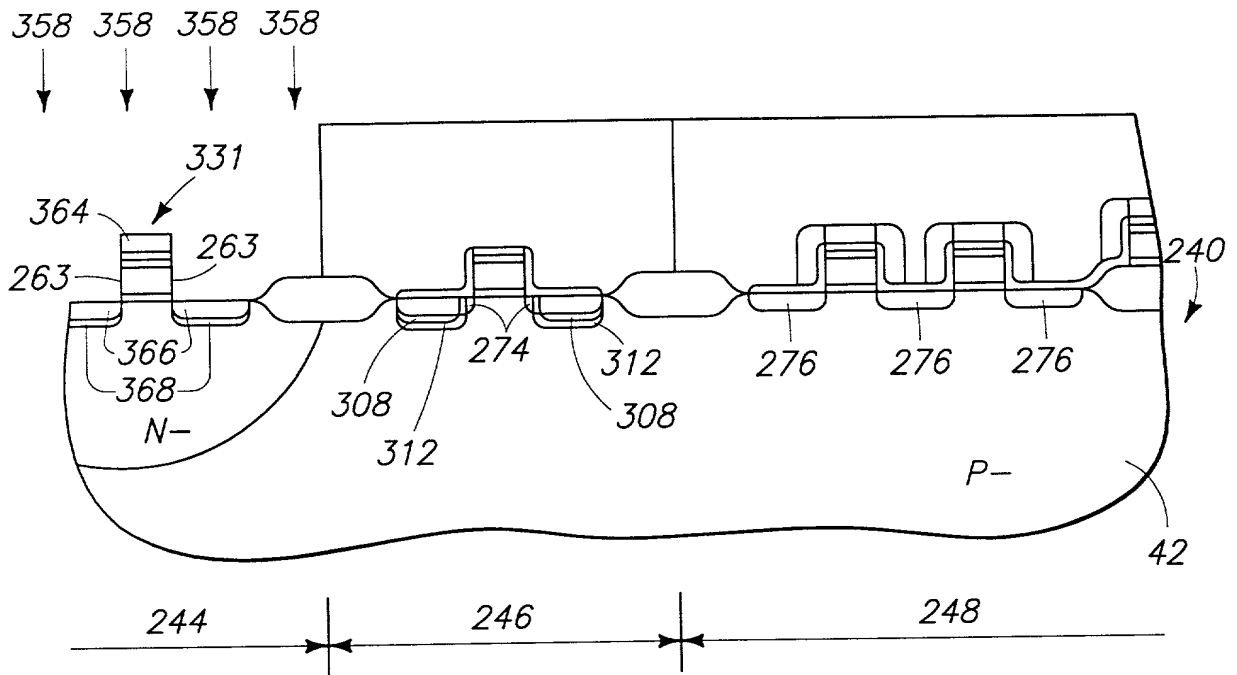


Fig. 19

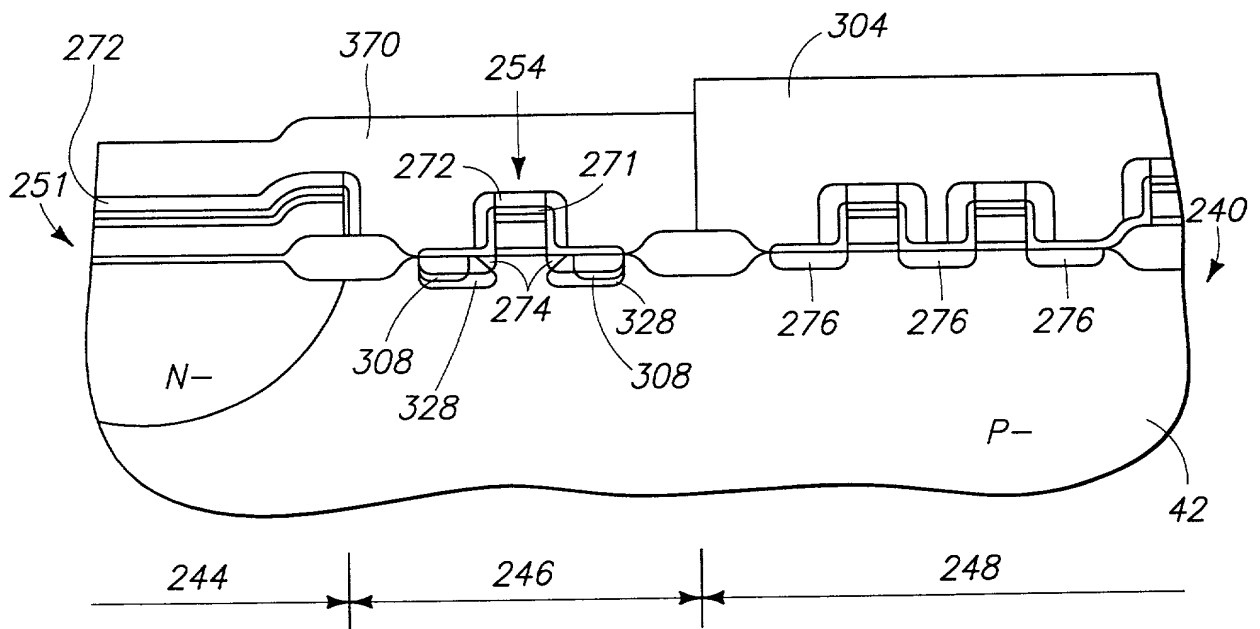
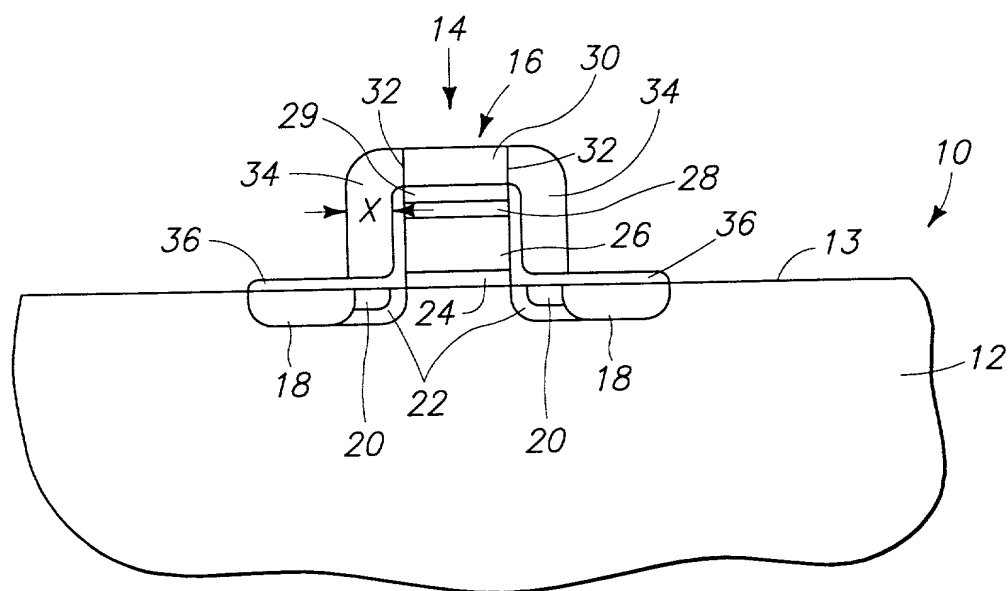
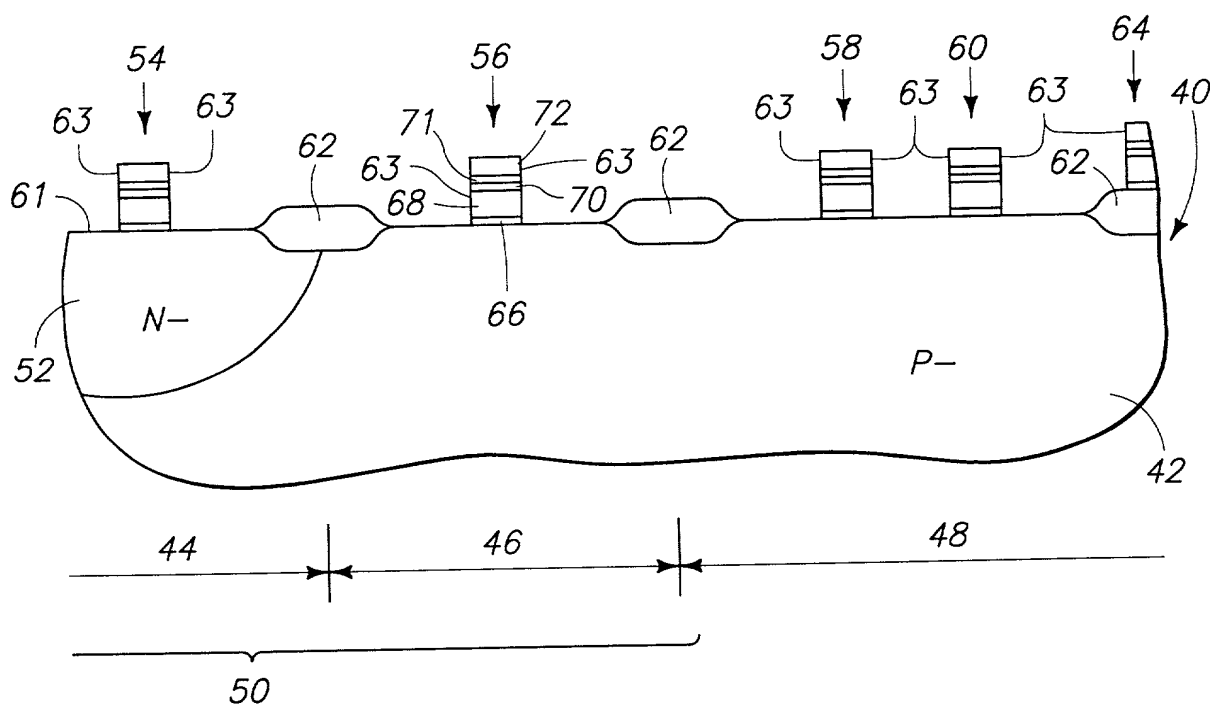


Fig. 20

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II II I
PRIOR ART



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PRIOR ART

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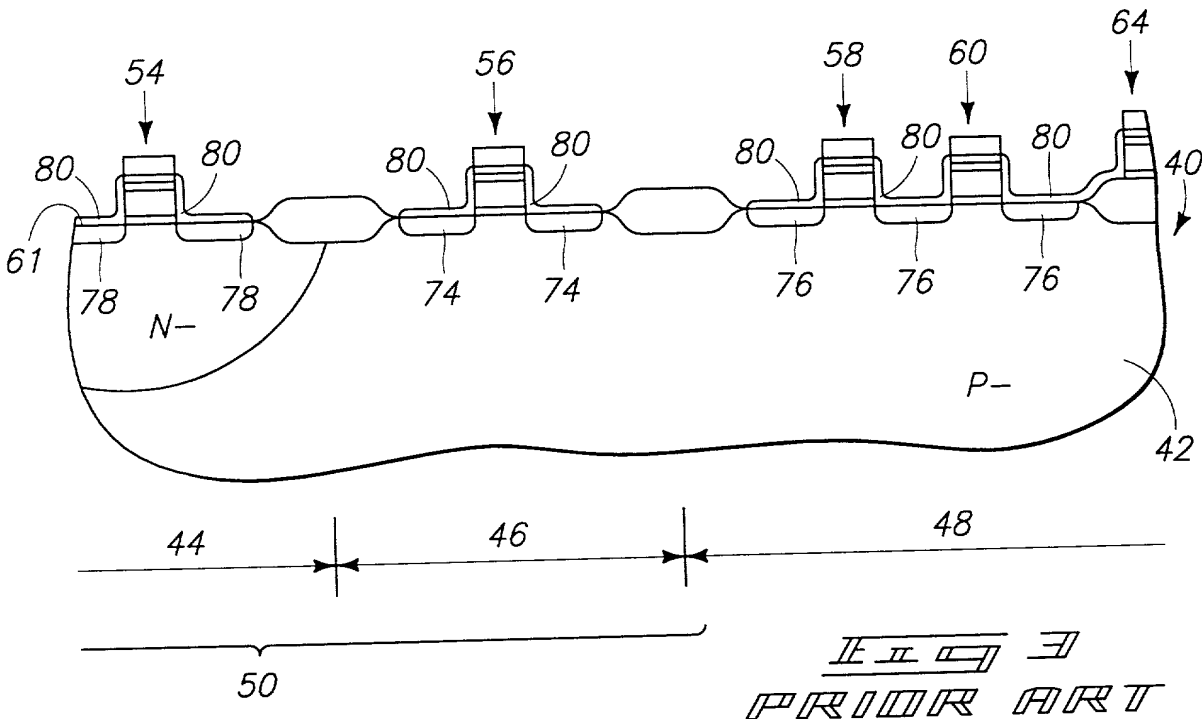


FIG 3
PRIOR ART

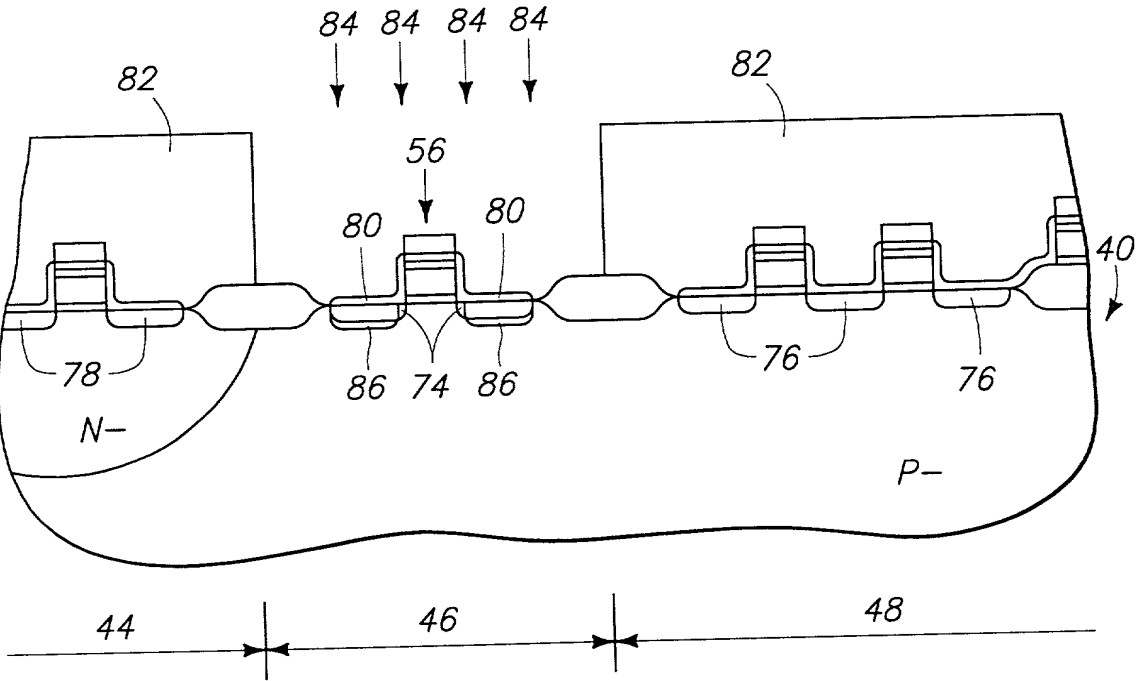


FIG 4
PRIOR ART

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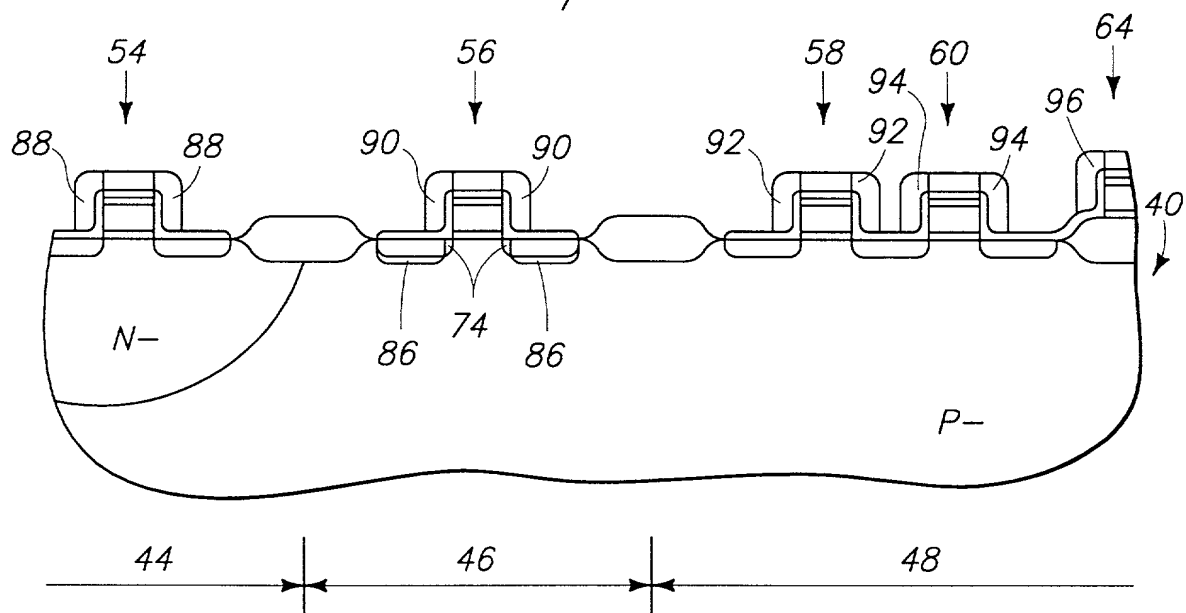


FIG 5
PRIOR ART

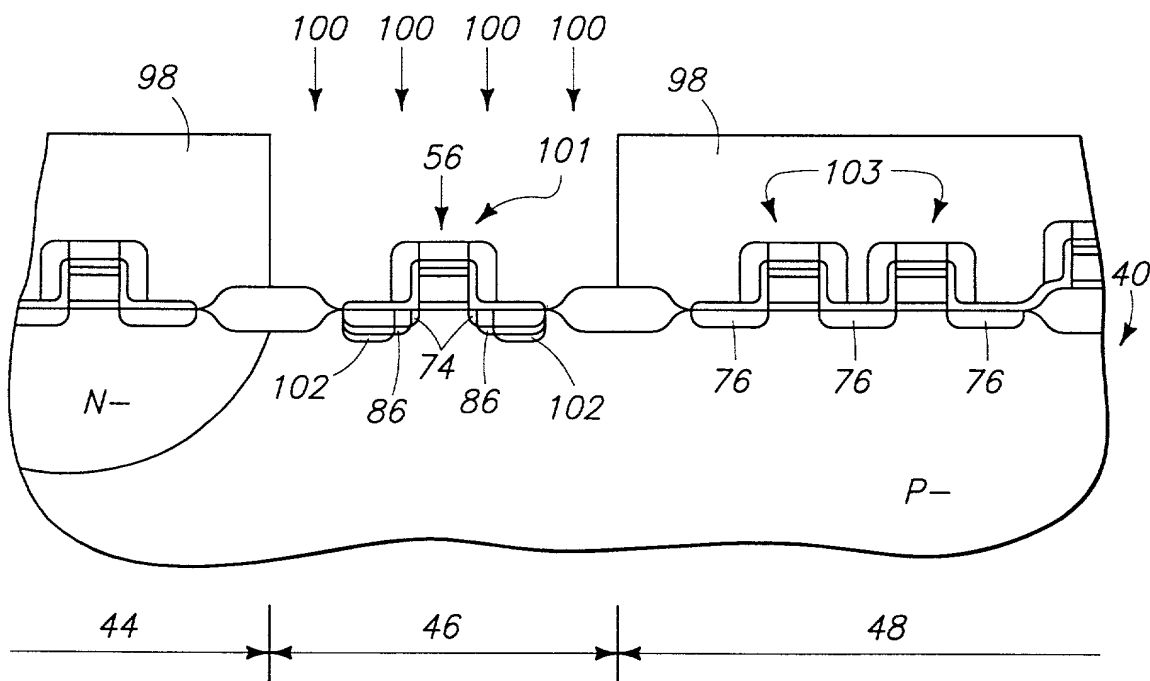
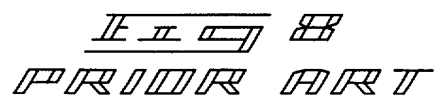
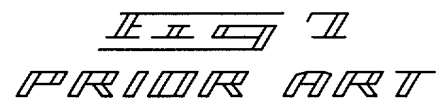


FIG 6
PRIOR ART

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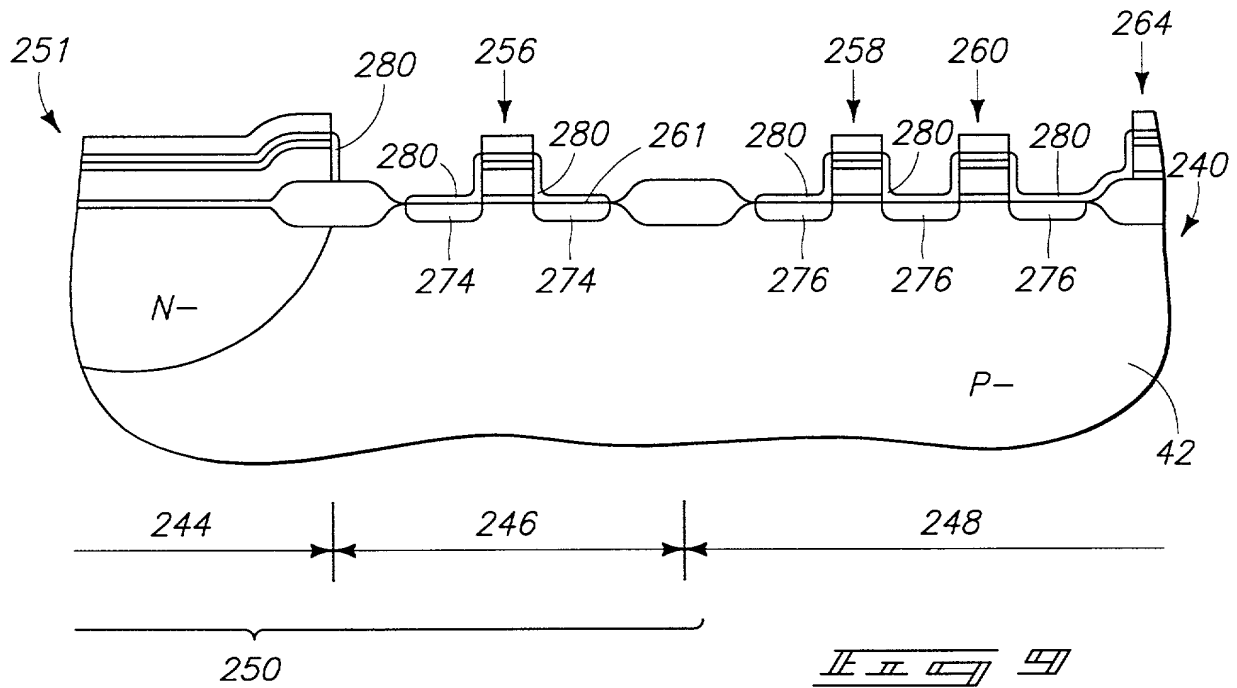


FIG. 1
PRIOR ART

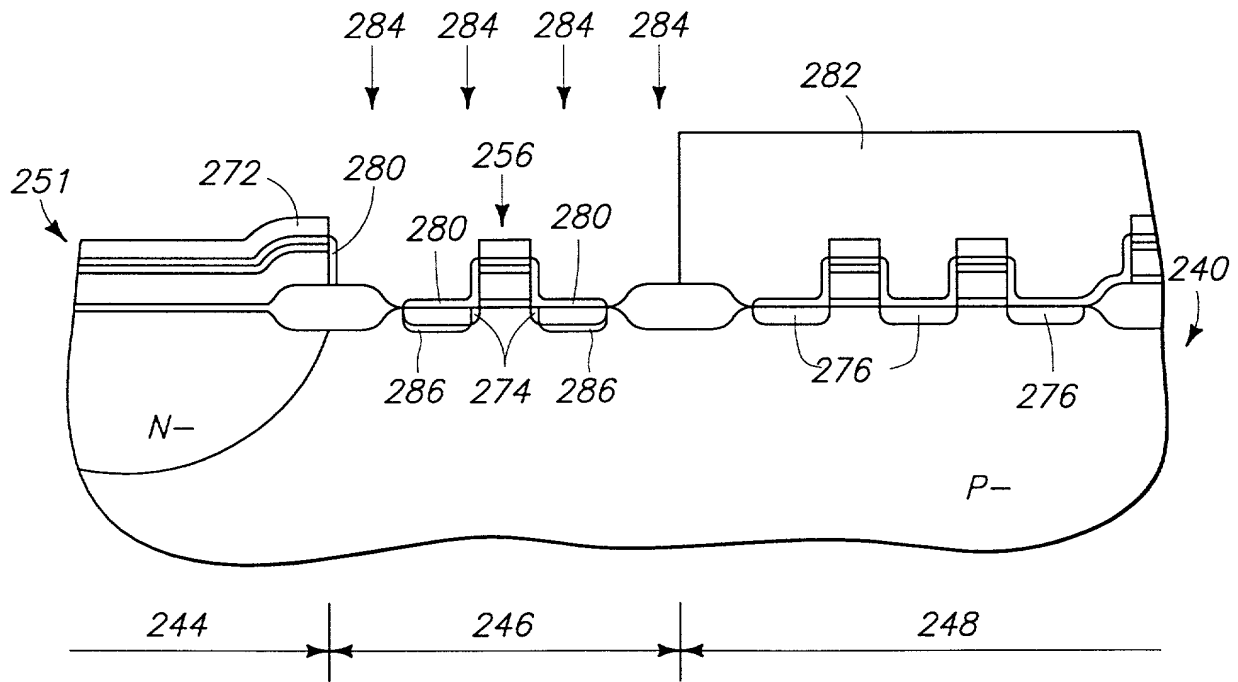


FIG. 2
PRIOR ART

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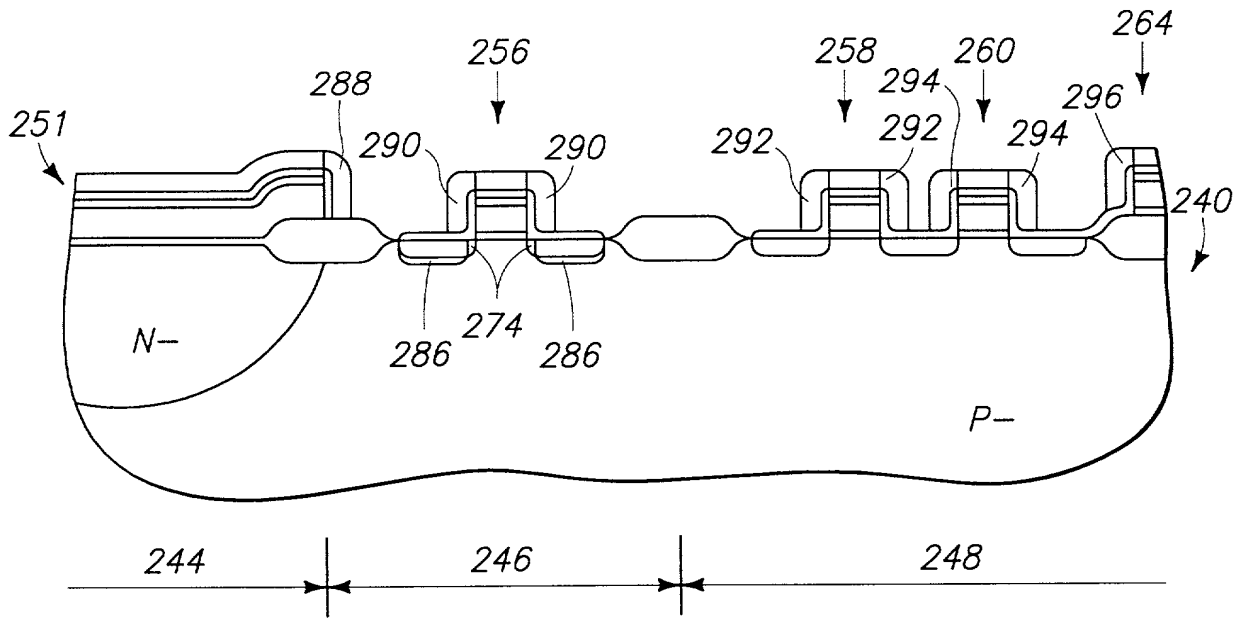


FIG. 1
PRIOR ART

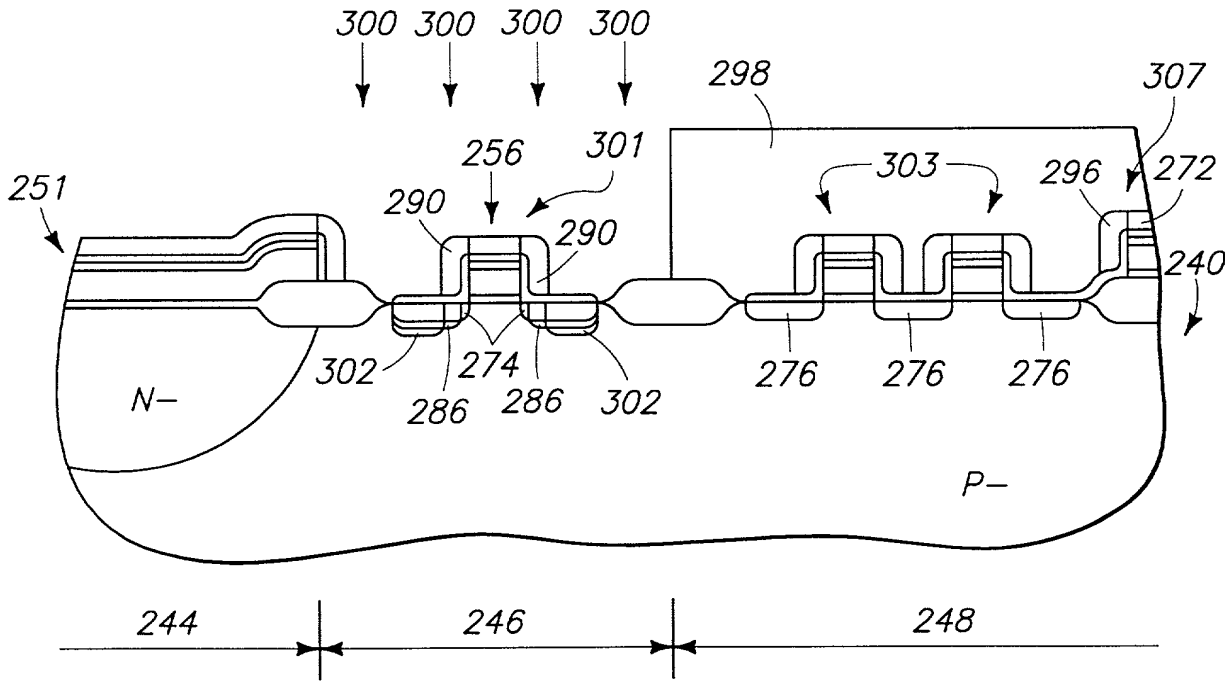
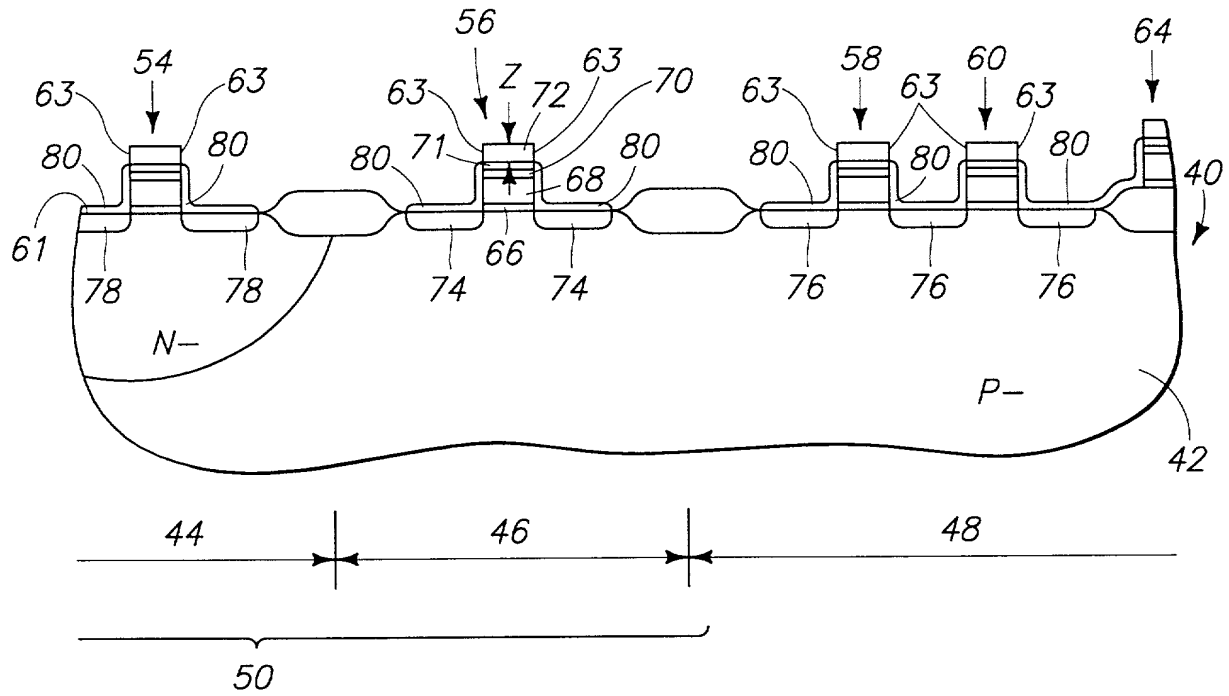
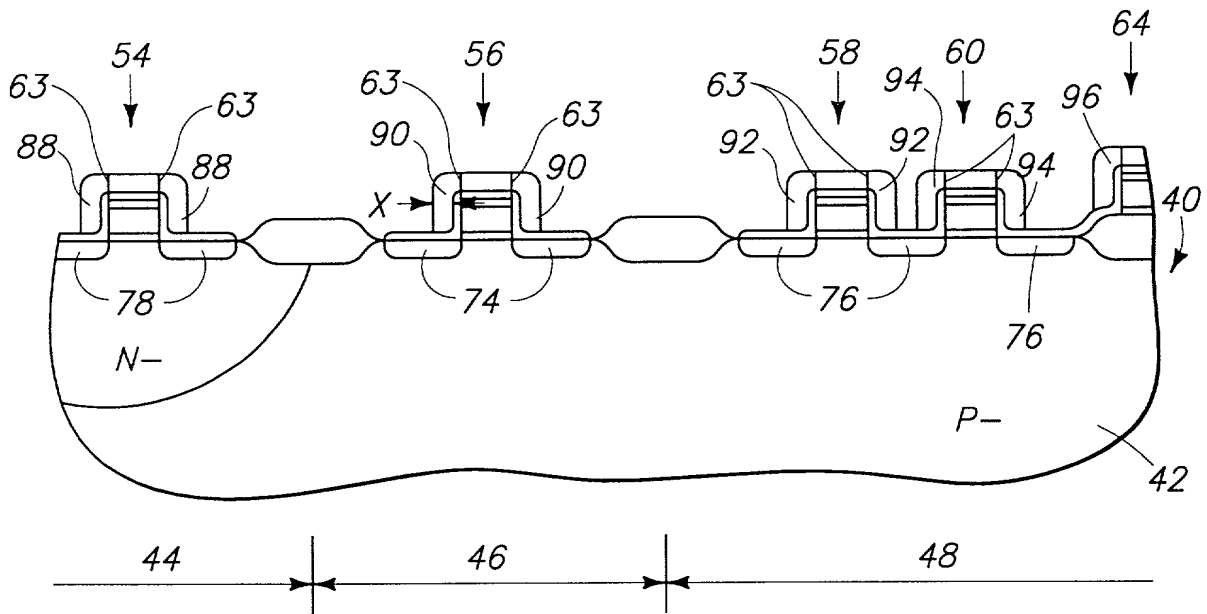


FIG. 2
PRIOR ART

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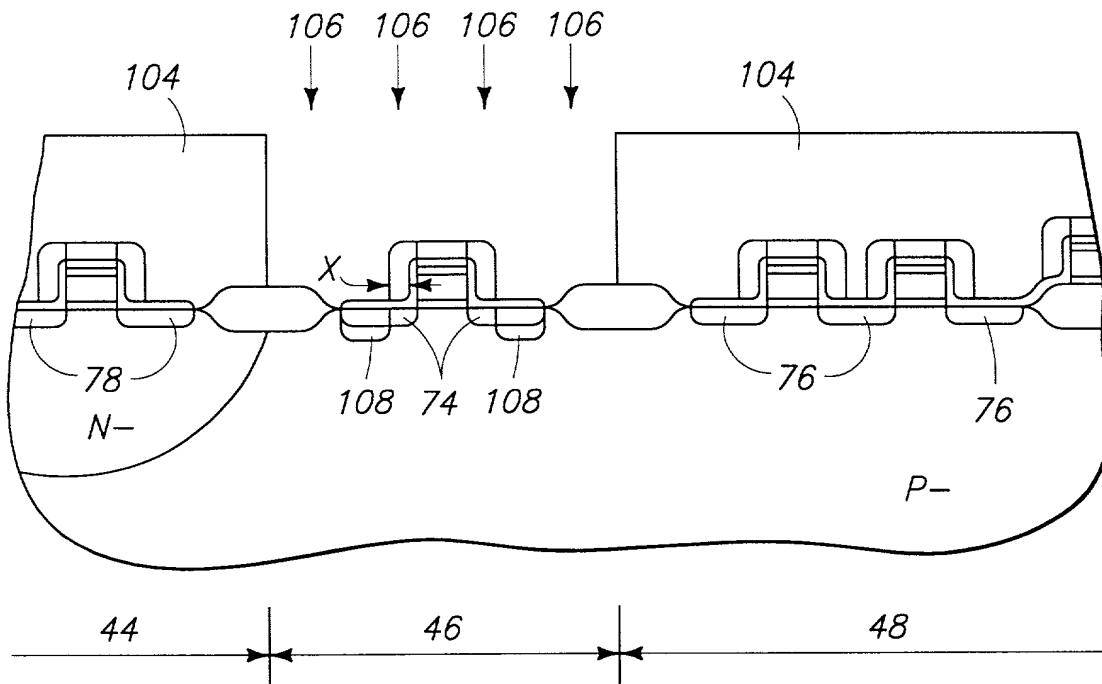


Fig. 15

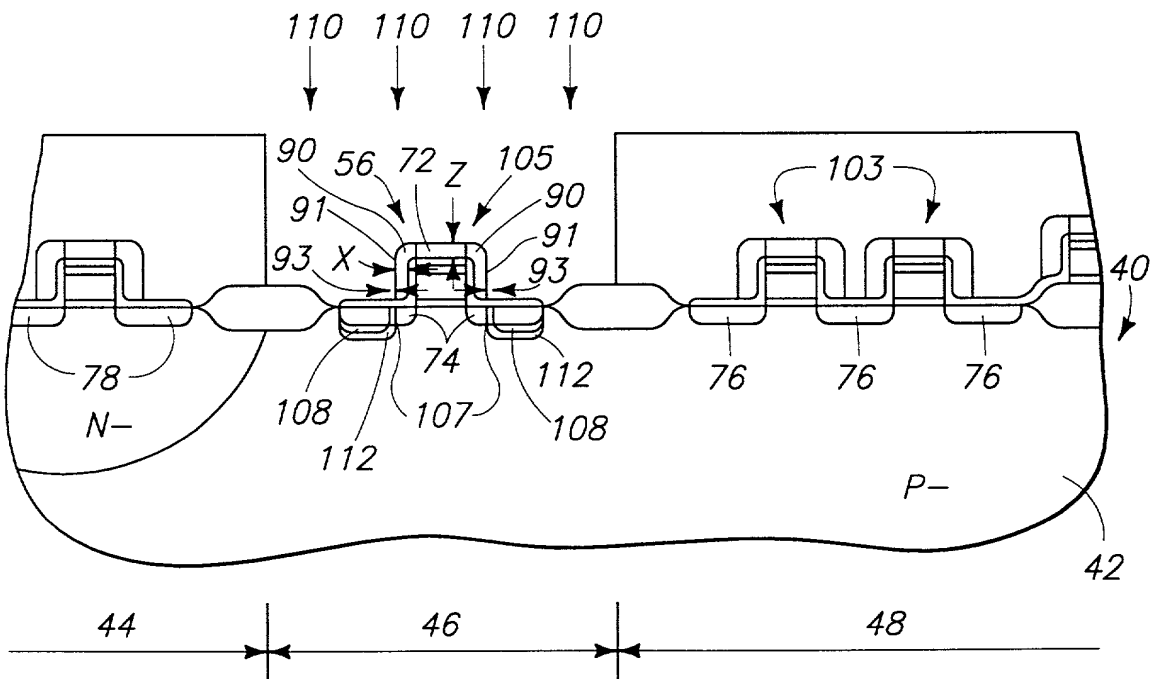


Fig. 16

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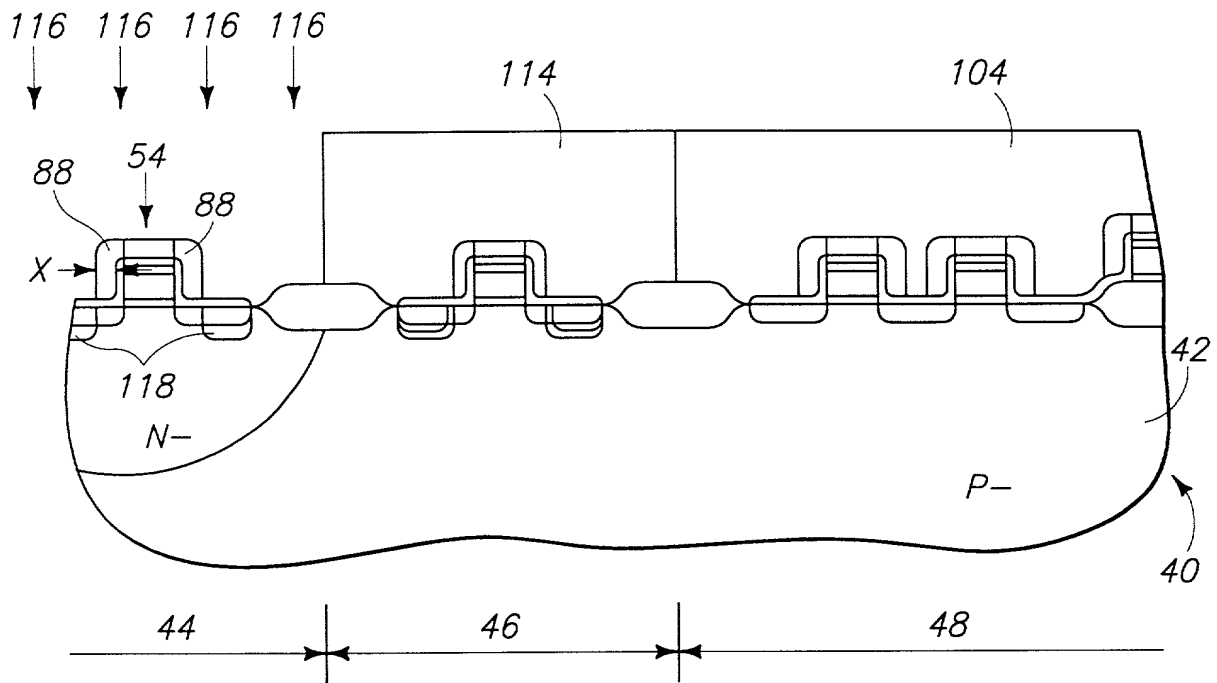


Fig. 11A

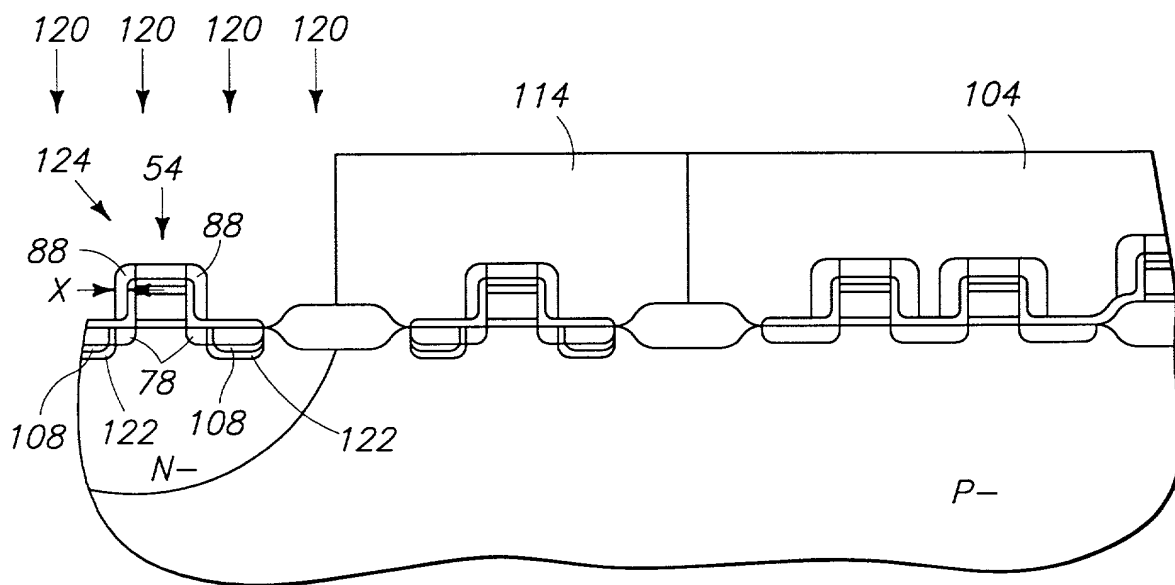


Fig. 11B

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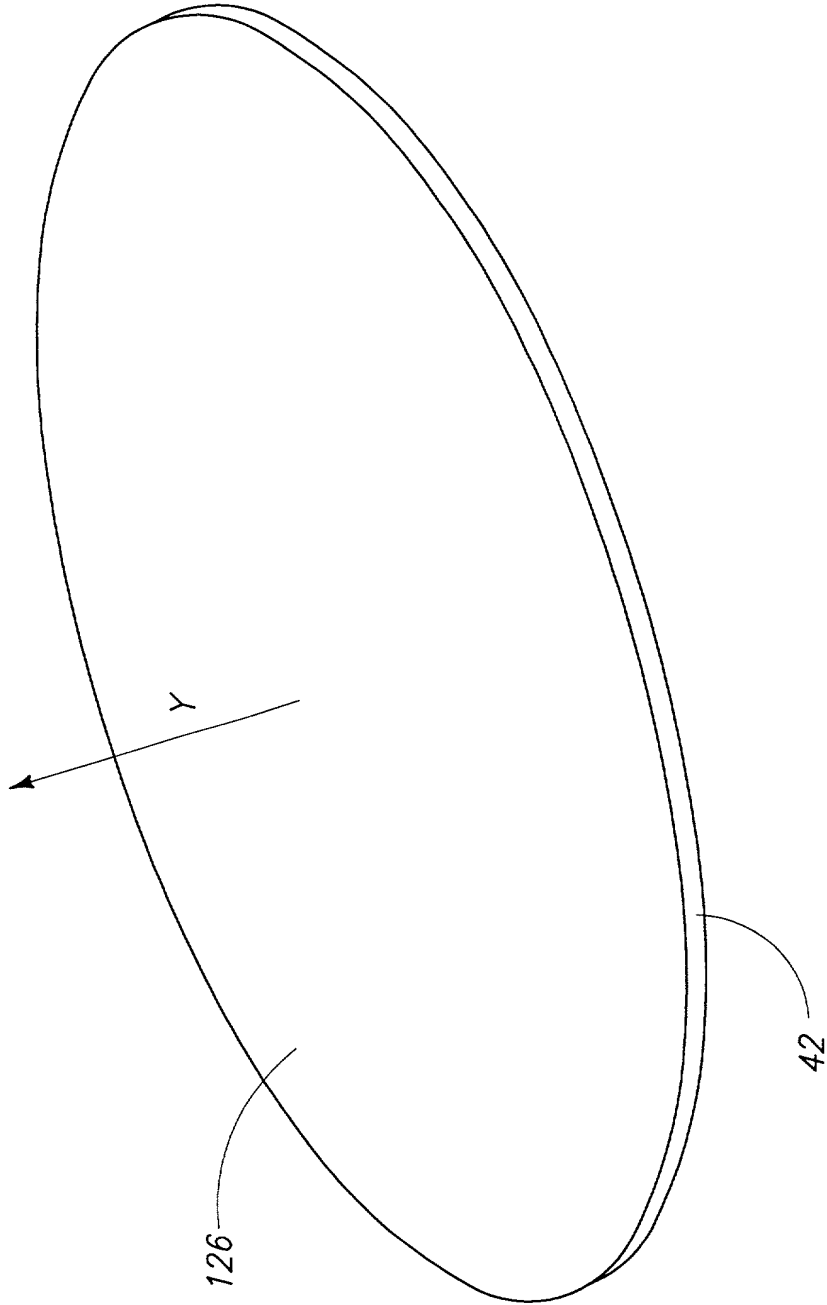


FIG. 10

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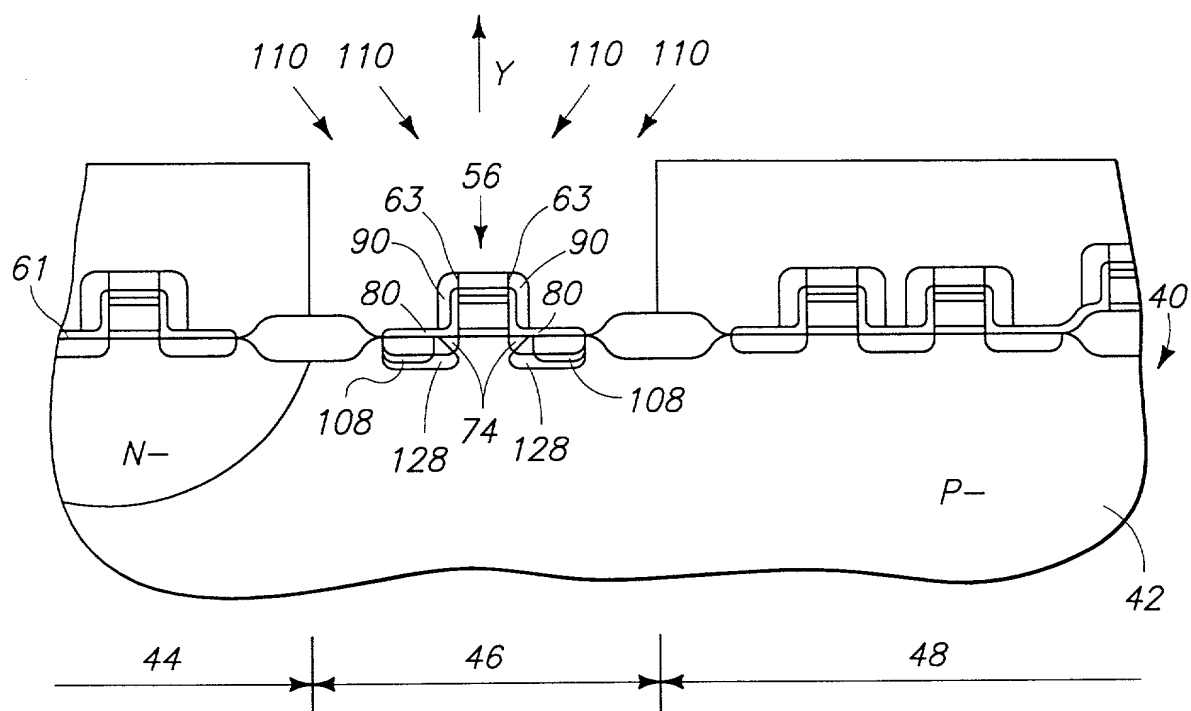


Fig. 11

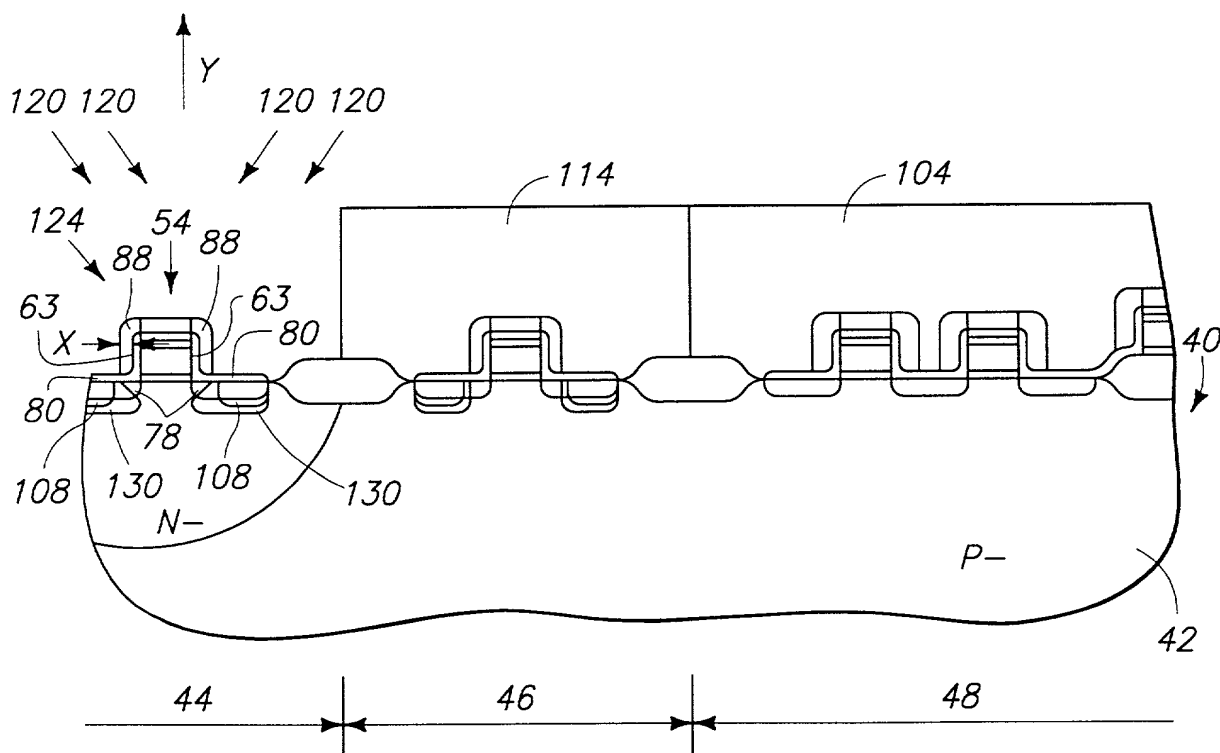


Fig. 12

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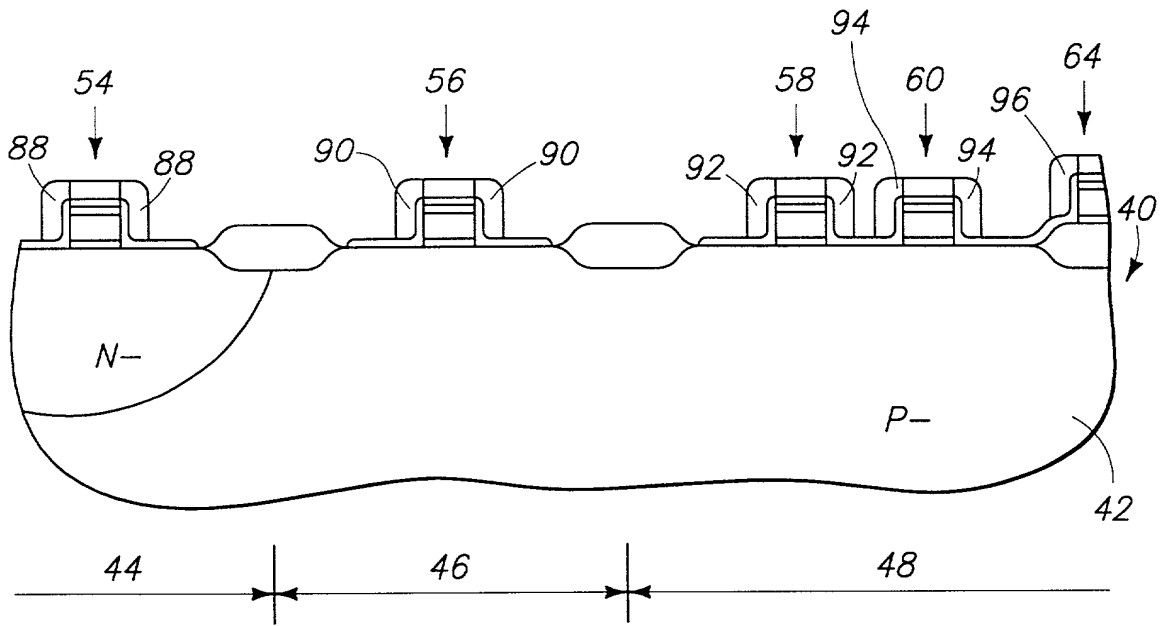


Fig. 22

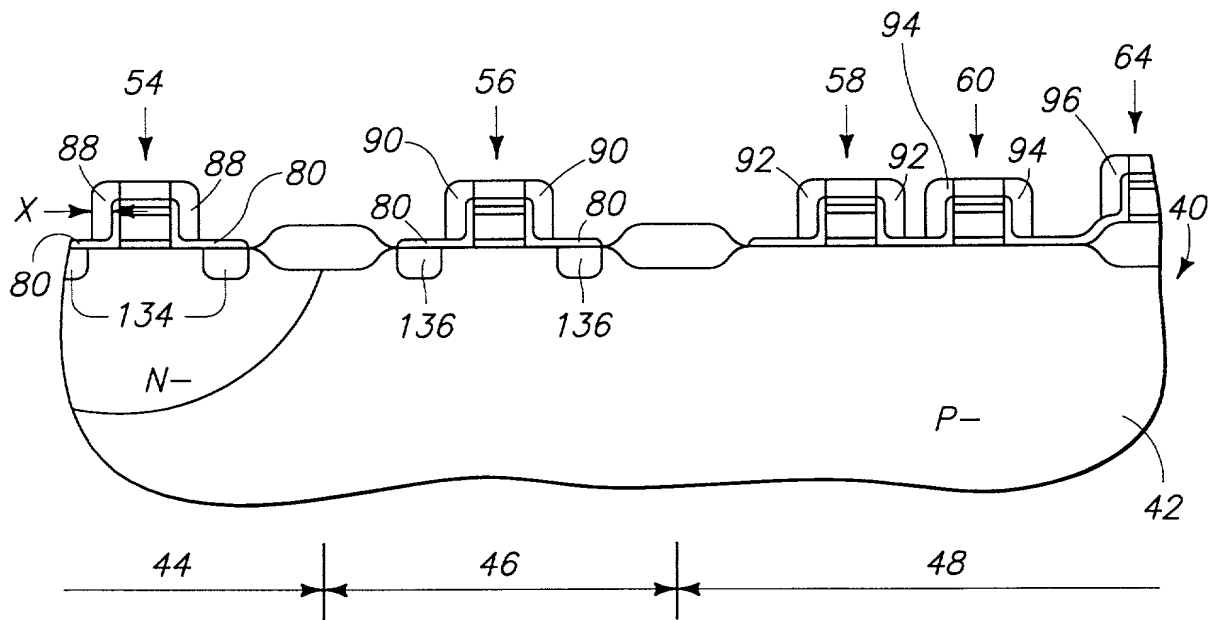
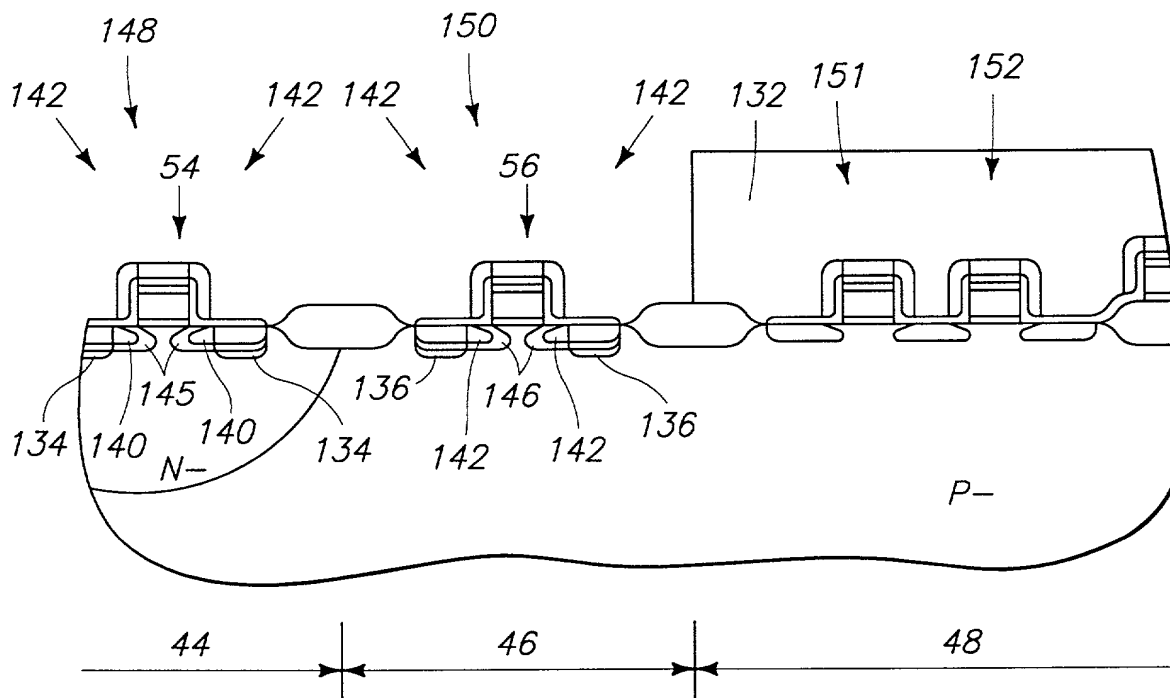
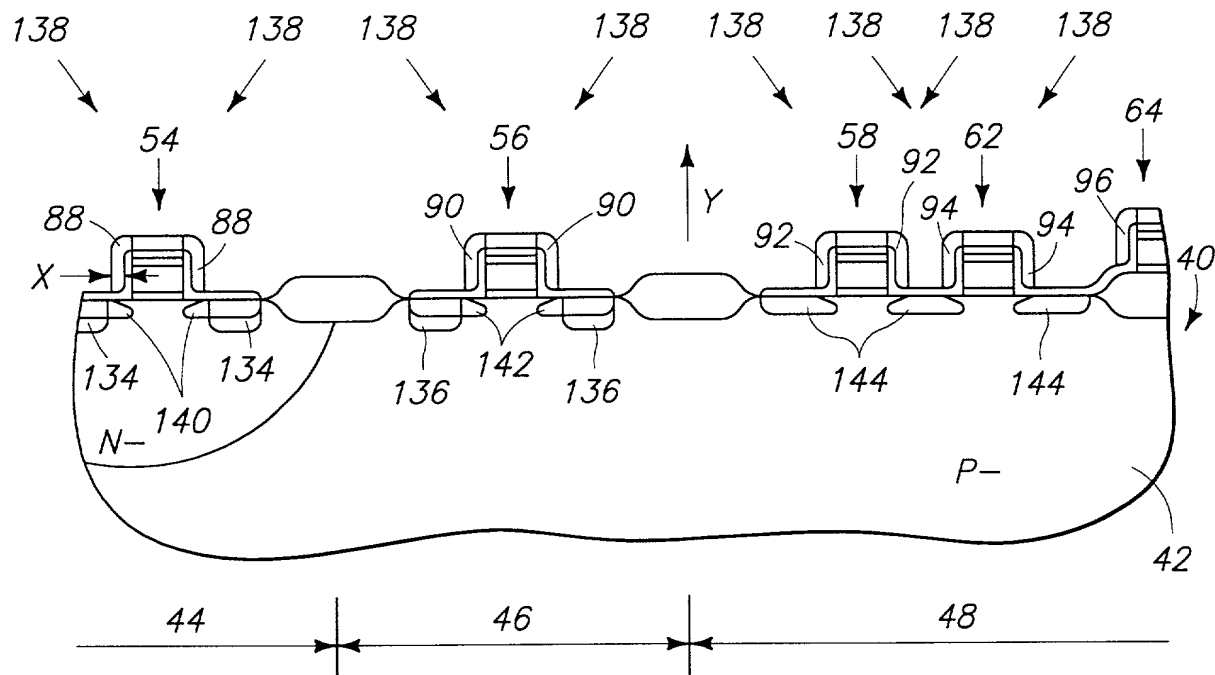
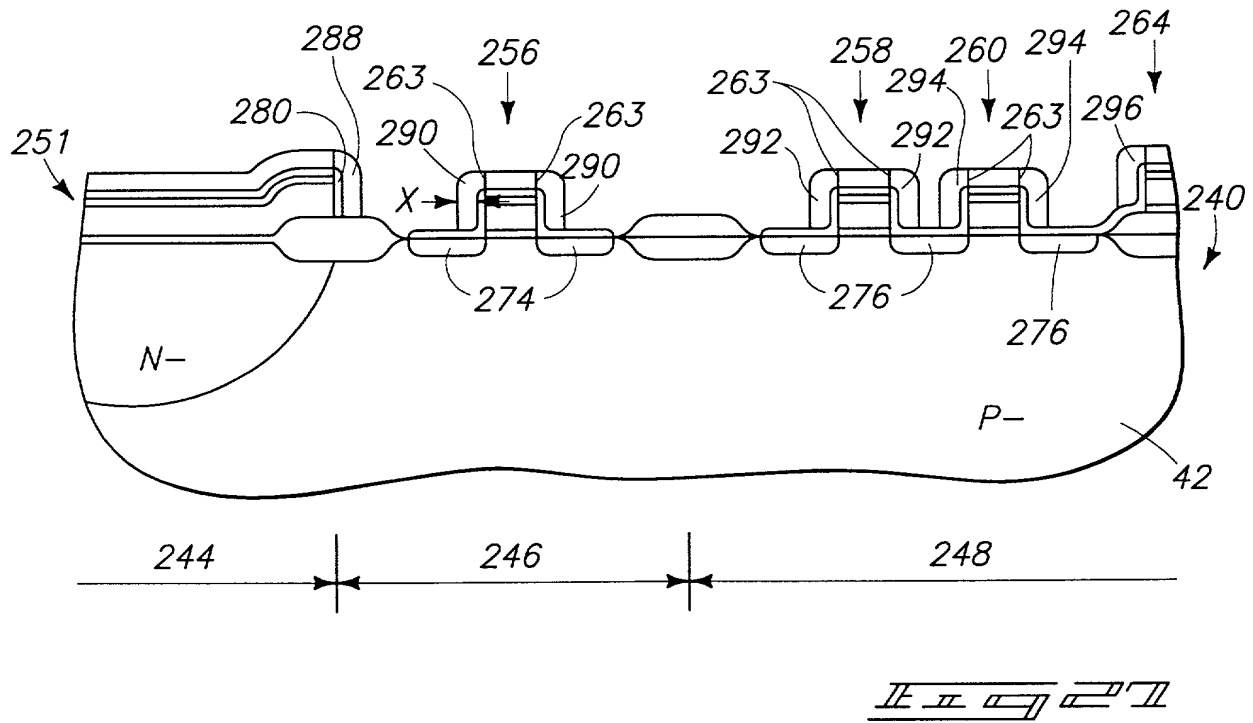
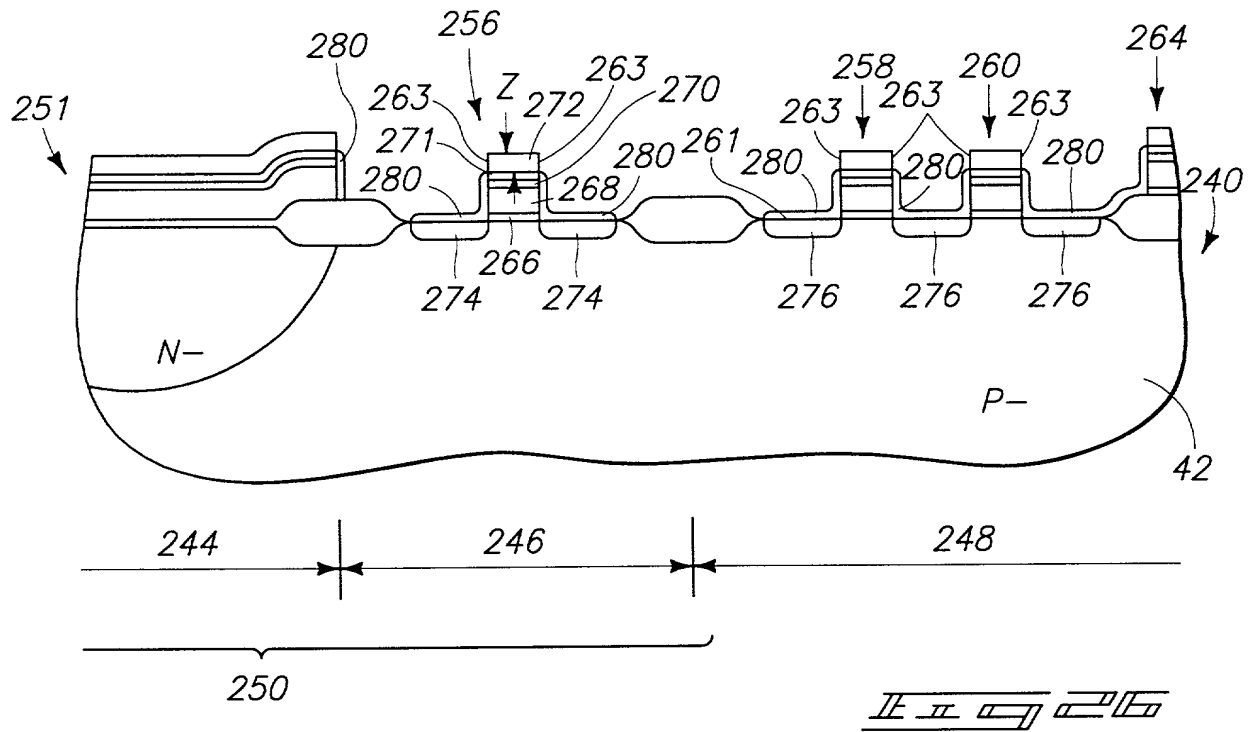


Fig. 23

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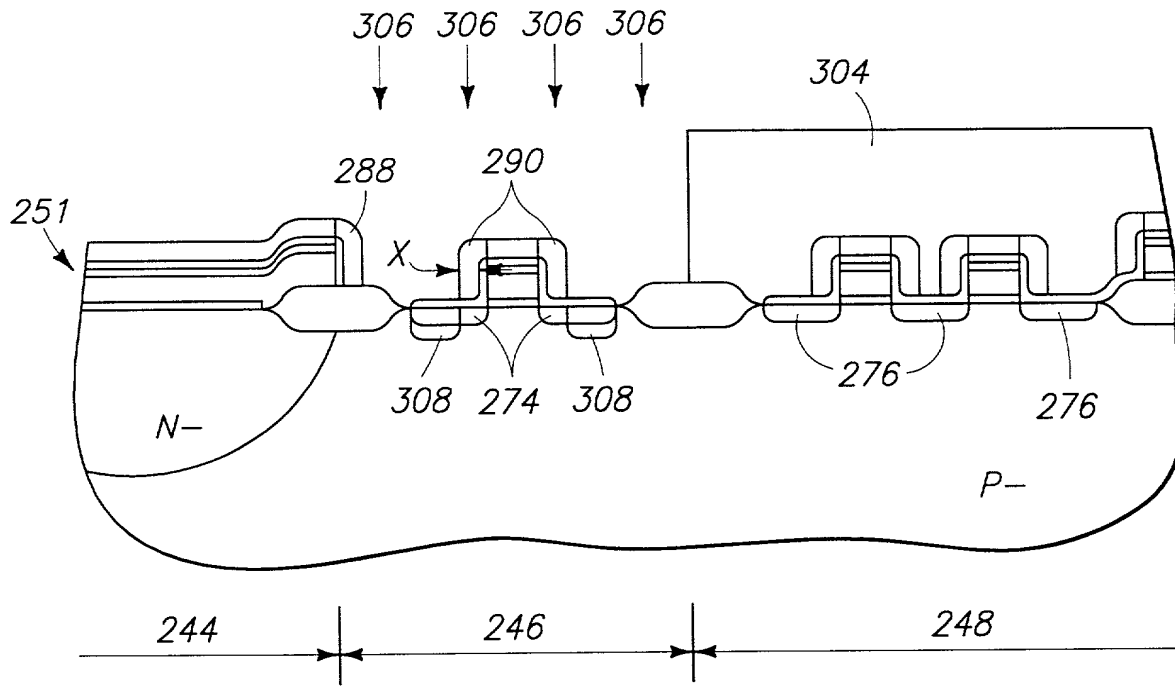


Fig. 28

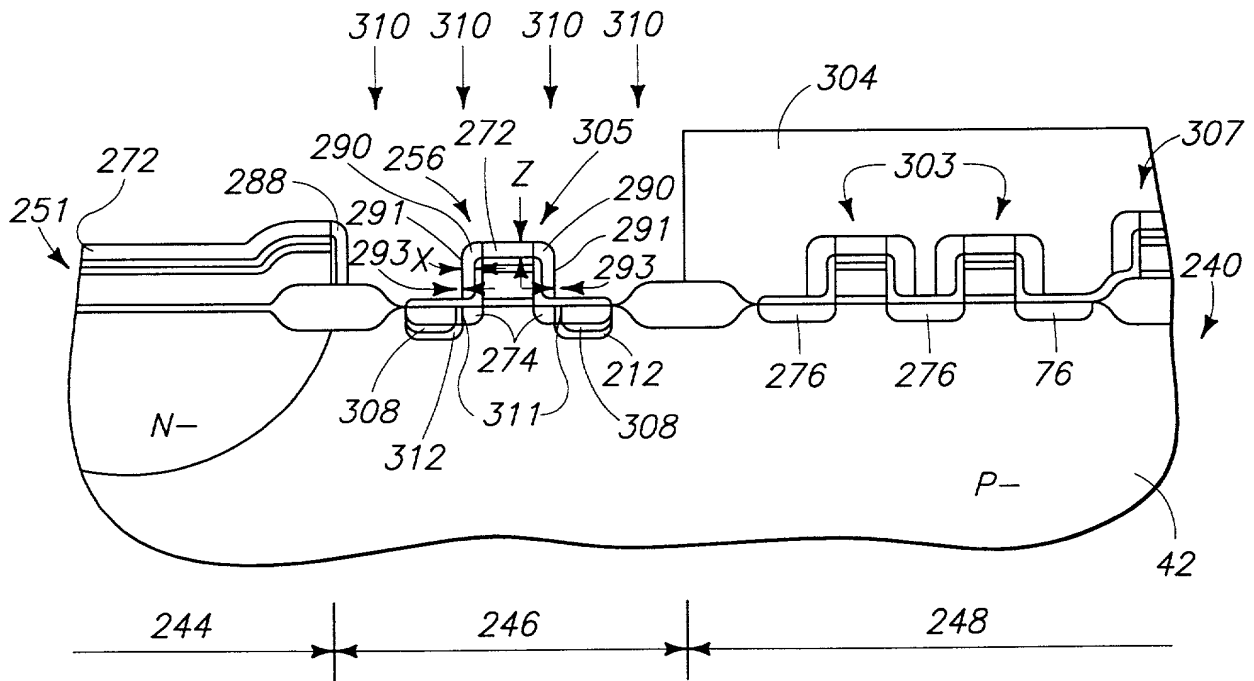
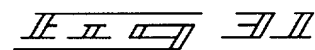
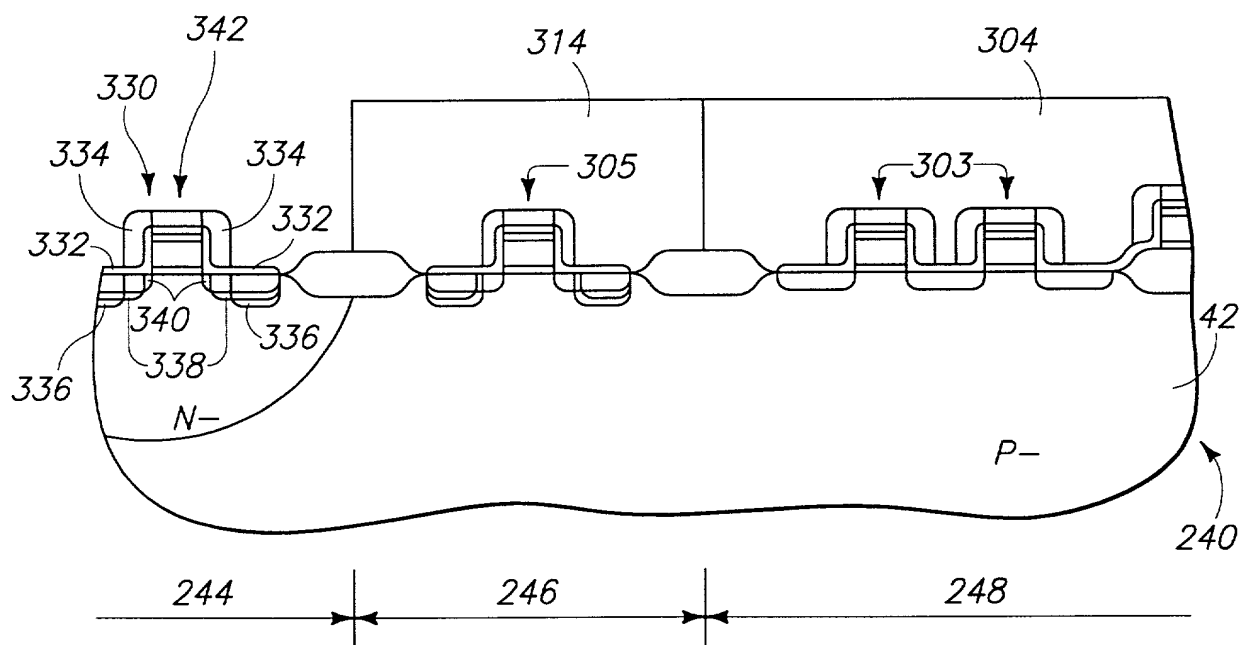
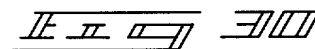
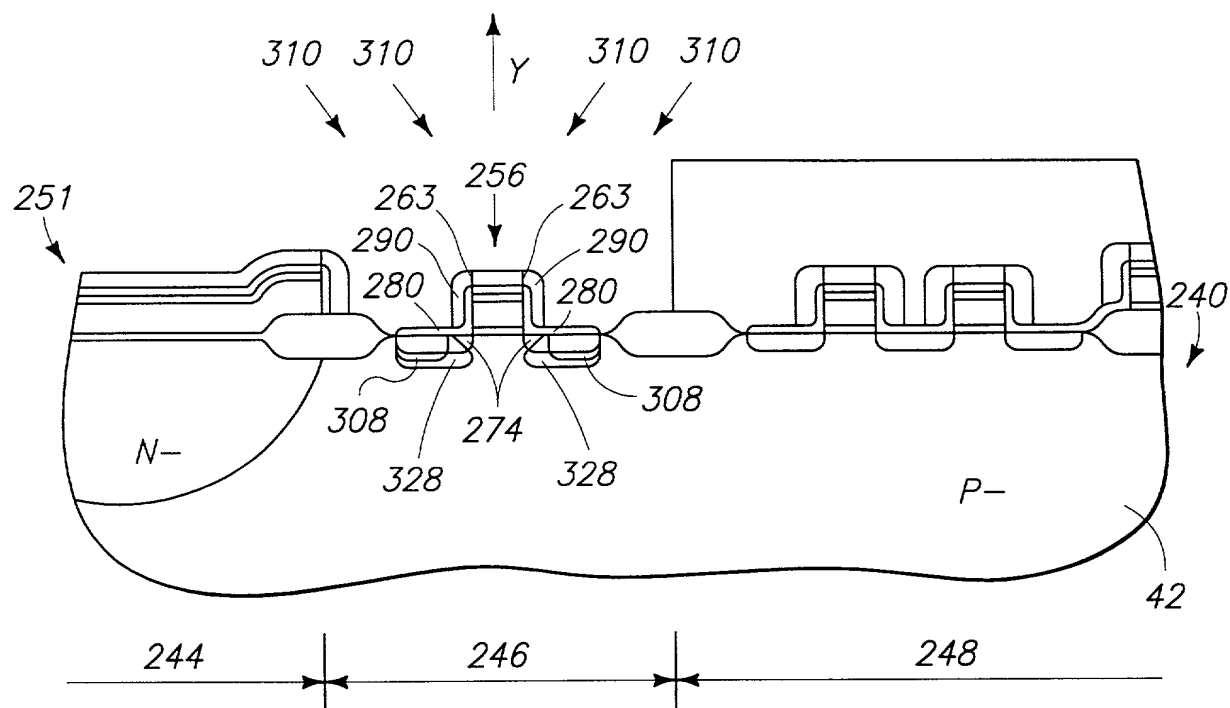


Fig. 29

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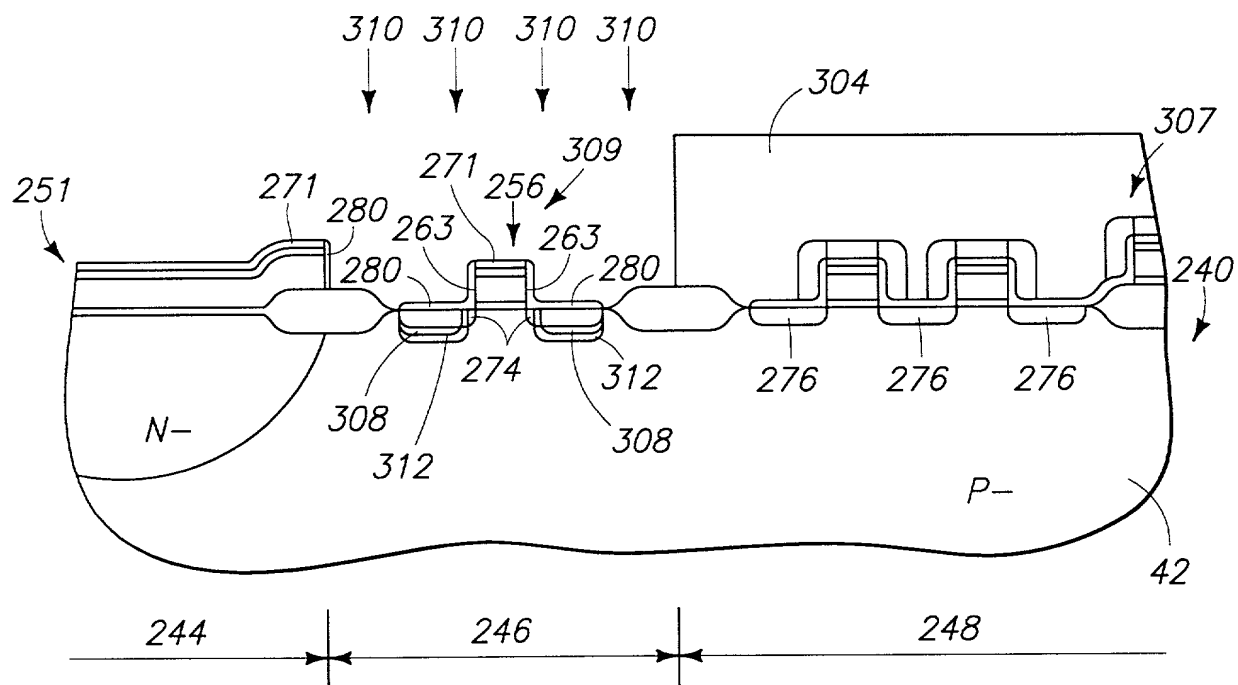


Fig. 17

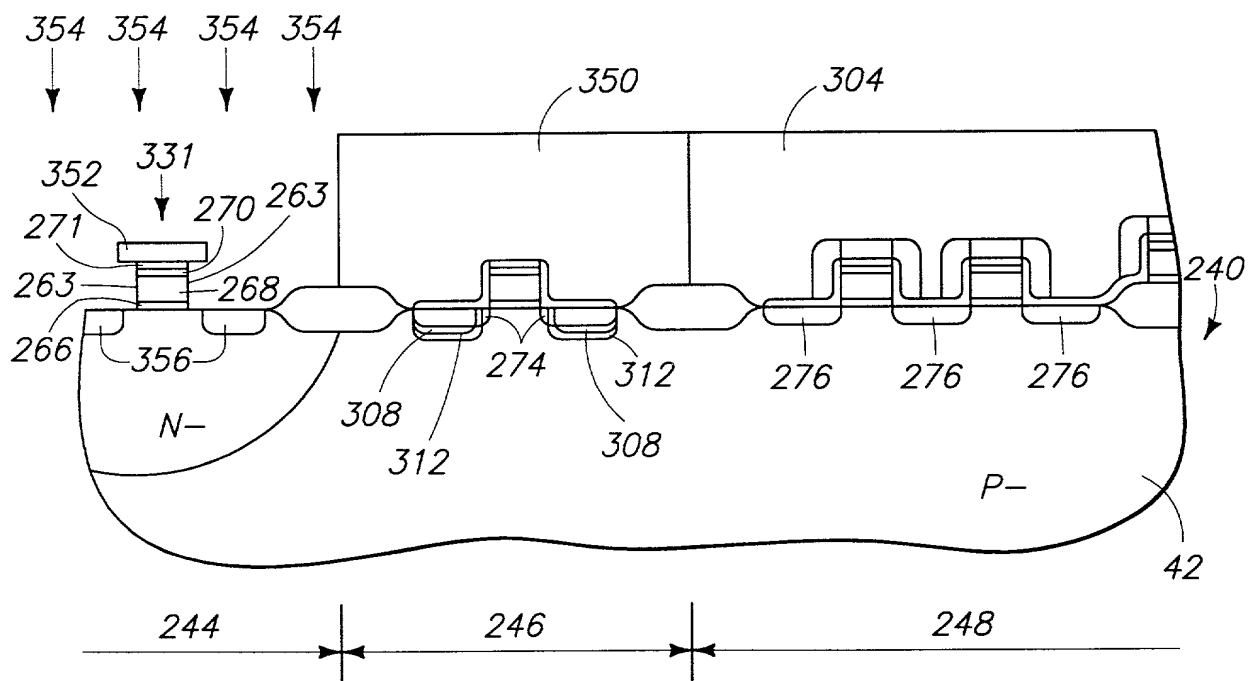


Fig. 18

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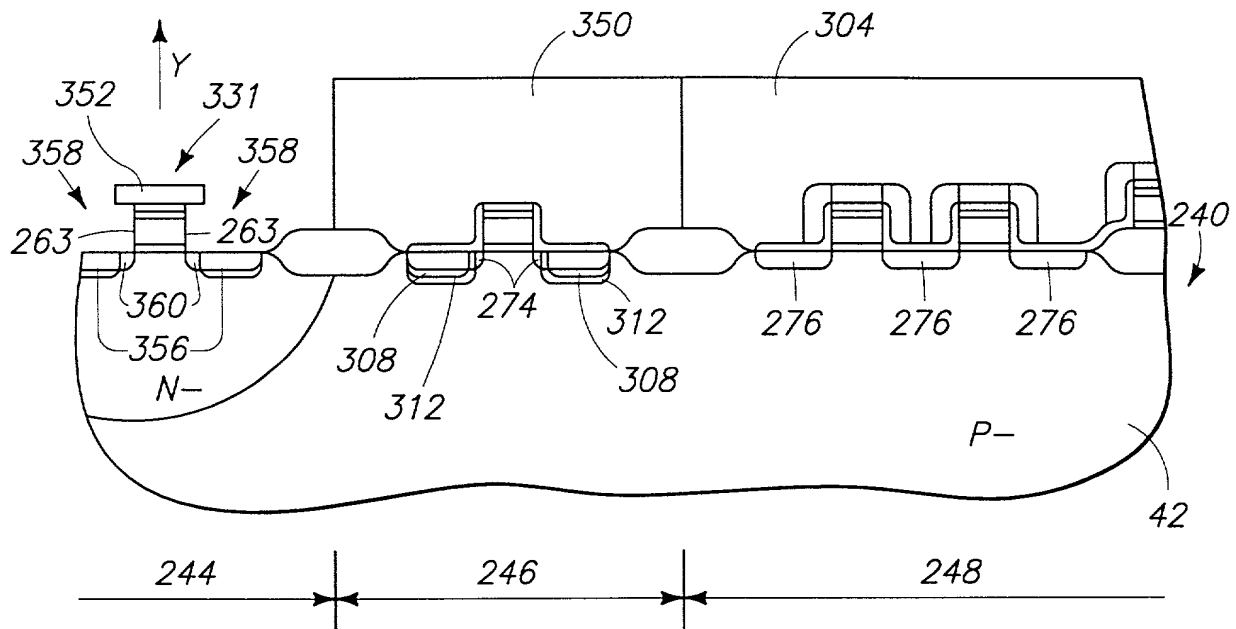


Figure 18

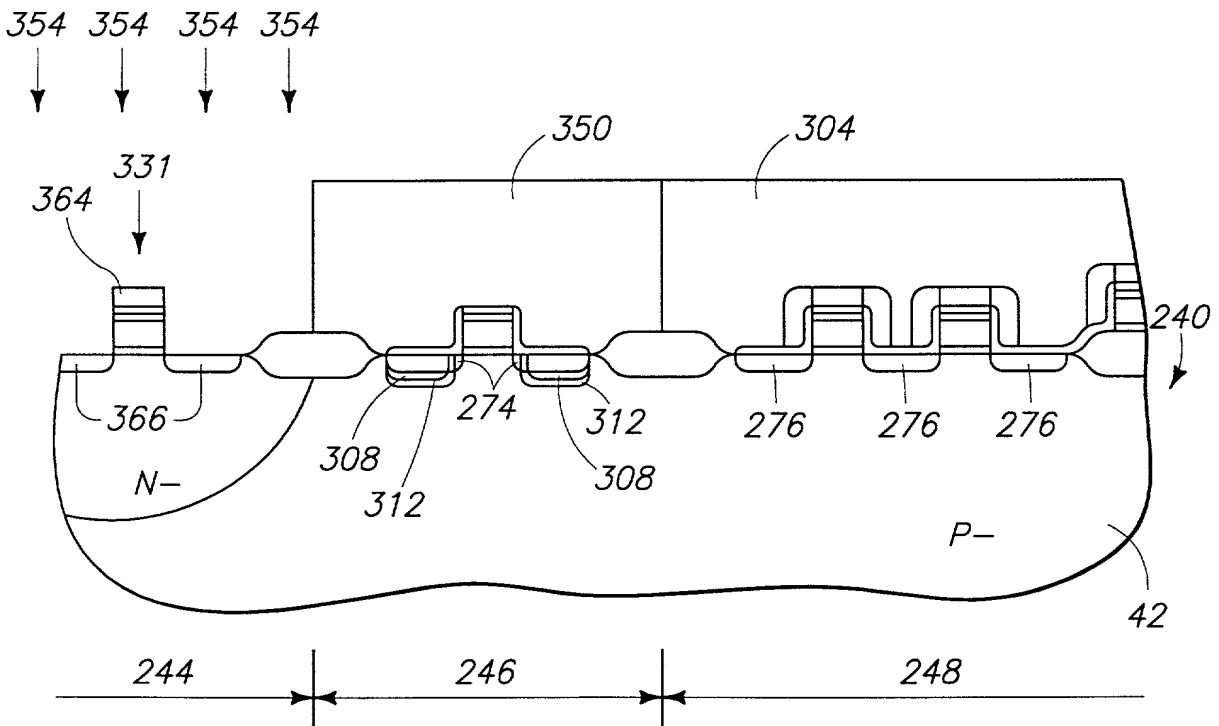


Figure 19

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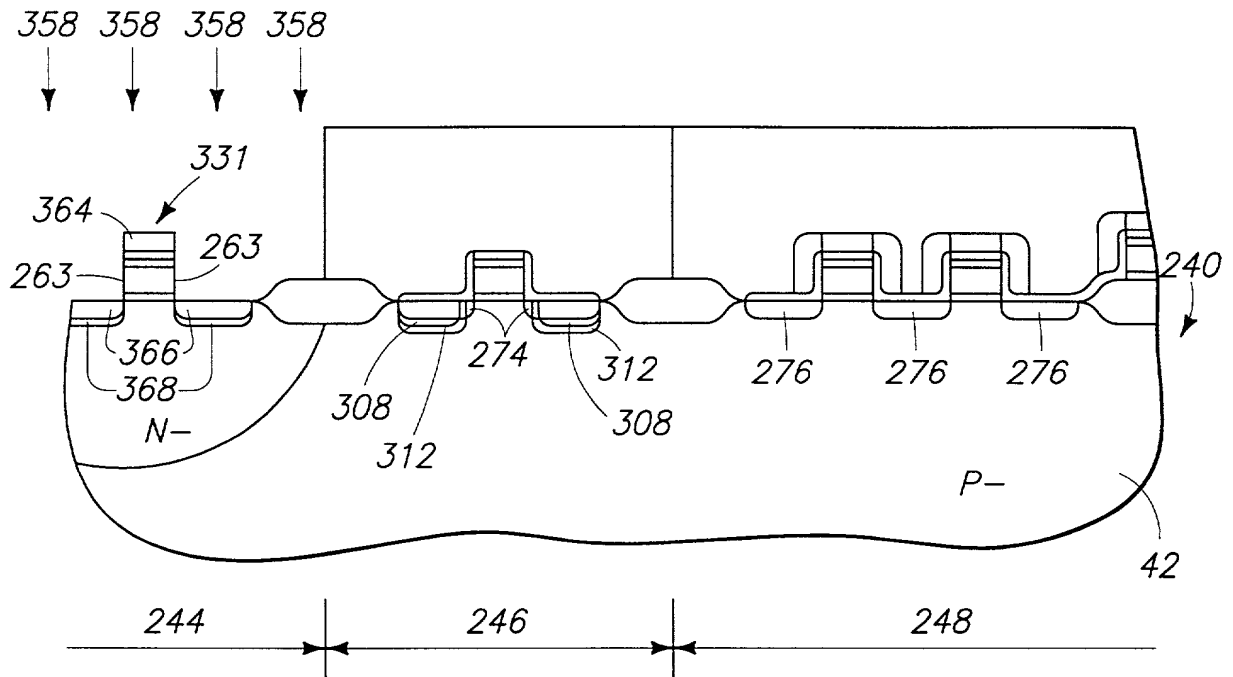


Fig. 20

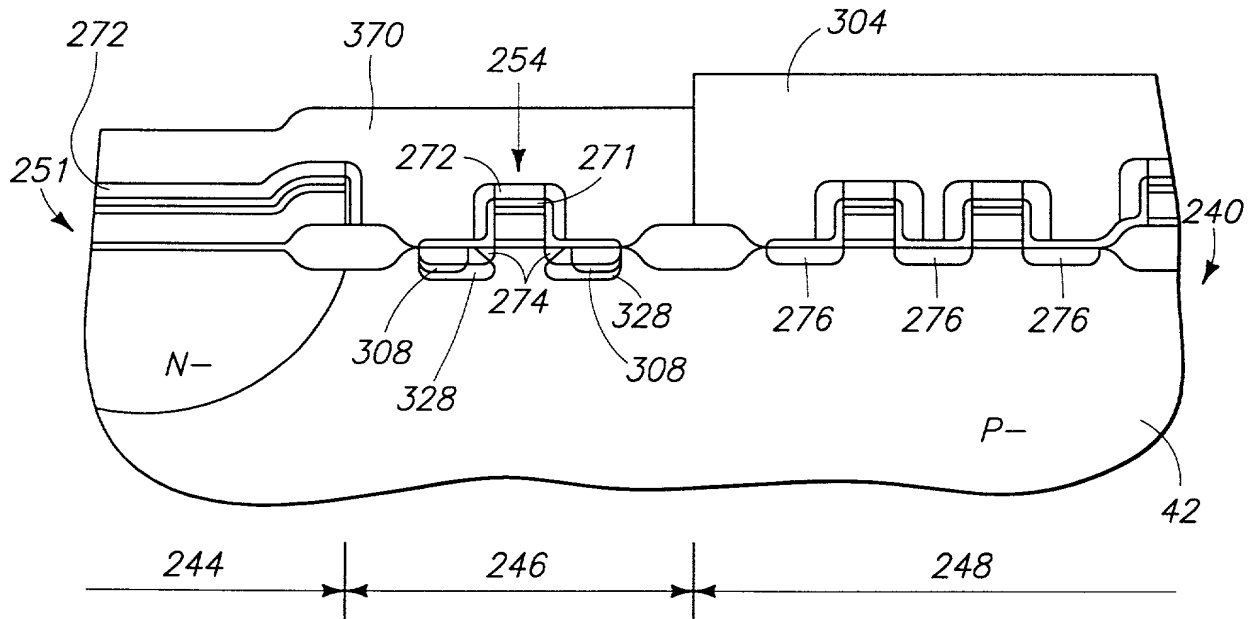


Fig. 21

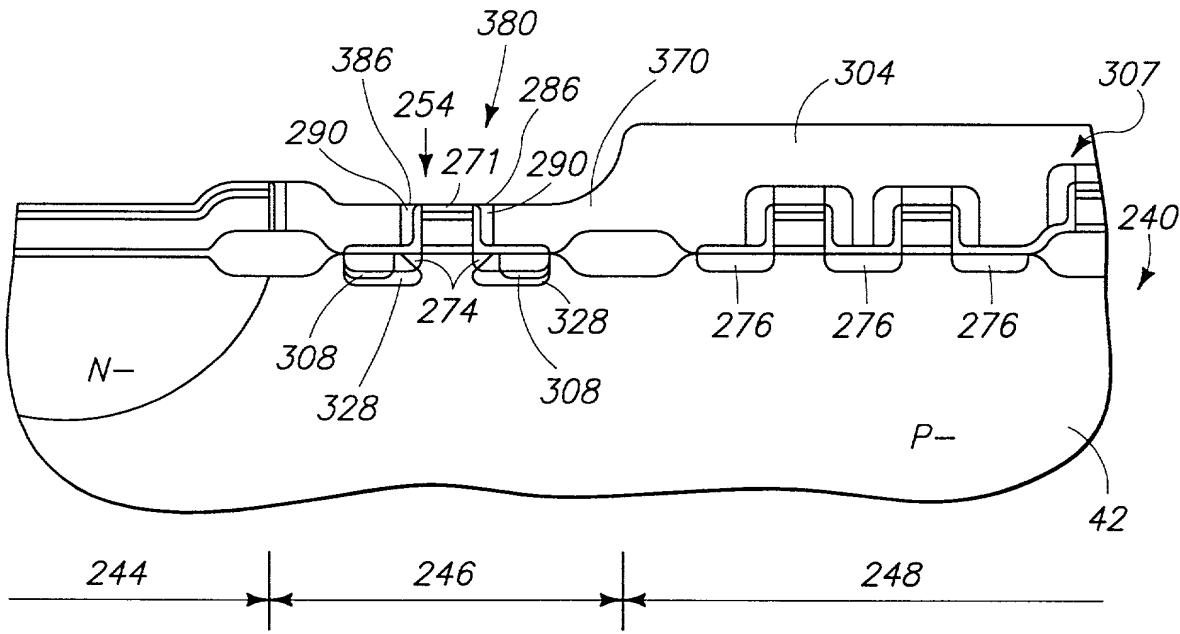


FIG. 20